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13. ABSTRACT (maximum 200 words)

This report presents the results of research on "compliant substrate" behavior in III-V semiconductors grown by molecular beam epitaxy (MBE) on thin (50-80Å) InGaAs layers on GaAs, and in II-VI semiconductors (HgCdTe, CdTe, ZnTe) grown on thin Si(211) layers on Si(100). A comprehensive experimental study was conducted utilizing spectroscopic ellipsometry, transmission electron microscopy, and atomic force microscopy at various stages in the fabrication and processing of the "compliant" layers and during MBE growth on those layers. Contrary to earlier reports by other investigators, we obtained no evidence for defect reduction or solid phase atomic rearrangement due to substrate "compliancy" in either of the III-V or II-VI systems studied here. We conclude that the early reports of compliancy may have been the erroneous interpretation of limited experimental data. Indeed, a theoretical consideration of stress relief mechanisms in semiconductor thin films suggests that many of the proposed compliancy mechanisms are not feasible. Although no evidence of substrate compliancy was obtained, we were nevertheless successful in growing high quality II-VI layers by MBE on thin Si(211) layers bonded to Si(100) substrates. This has important implications for monolithic integration of HgCdTe infrared focal plane arrays with readout circuitry fabricated in Si(100) substrates.

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Section 1
INTRODUCTION

Over the past decade there have been several reports in the literature suggesting that ultra-thin (<60 Å) layers can effectively function as "compliant" substrates capable of mitigating defect formation and propagation in heteroepitaxial growth of lattice mismatched structures. For example, it has been proposed that compliant substrates formed by a process called "twist-bonding" may be the essential ingredient in ultimately realizing the epitaxial growth of "anything-on-anything" – the Holy Grail in the field of epitaxial materials science and substrate engineering. The successful implementation of this technology would have significant implications for improving the quality of heteroepitaxial growth and heterogeneous integration of disparate semiconductor materials for high performance microelectronics, photonics, and sensor arrays. In this program we have conducted a detailed experimental study of the validity and applicability of the compliant substrate concept within the context of two technologically relevant semiconductor materials systems, including III-V layers on GaAs, and II-VI materials on Si. Specifically, there were two principal technical objectives of this program: 1) to explore and demonstrate the use of "twist-bonded" compliant substrates for growth of Sb-based (6.1Å) semiconductor device structures on InGaAs-GaAs by molecular beam epitaxy (MBE), and 2) to develop Si(211) interlayers that facilitate the MBE growth of II-VI materials (e.g. CdTe, HgCdTe) with low defect densities on Si(100) substrates.

The first objective addresses the expressed need within the III-V photonics and microelectronics communities for a "universal substrate" that can replace smaller, more costly substrates such as GaSb that are not available in semi-insulating form for vapor-phase growth of high performance device structures. The second objective relates to an extremely important, but elusive goal in the development of large format, high performance infrared (IR) focal plane arrays for both staring and scanning IR detector applications. Cooled focal plane arrays are presently fabricated in HgCdTe epitaxial layers grown either on CdZnTe or Si(211) substrates. However, the readout electronics that process the output from each detector pixel are fabricated in Si(100) substrates. It is highly desirable to combine the readout electronics fabricated in the (100) material and the detector structures grown on the (211) material in a monolithically integrated way on the readout substrate. In this program we developed the methods for preparing a thin Si(211) "compliant" layer on a Si(100) substrate, and we evaluated the use of this Si(211)/Si(100) composite substrate for growth of II-VI epitaxial layers with reduced defect density.

This work was conducted by a team comprising researchers from HRL Laboratories (HRL – G.L. Olson, J.A. Roth, T.J. de Lyon, and J.E. Jensen) and The University of California at Santa Barbara (UCSB – Prof. J.S. Speck and his research group). HRL Laboratories served as the lead organization on the program and was responsible for technical activities that included *ex situ*

analysis of InGaAs-on-GaAs and Si(211)-on-Si(100) "compliant" layers, MBE growth and *in situ* analysis of epitaxial layers grown on the "compliant" substrates, and post-growth characterization of the composite structures. Investigators at UCSB performed transmission electron microscopy and atomic force microscopy characterization of III-V and Si-based compliant substrate structures, analyzed defect properties in the materials, and made significant contributions to the elucidation of mechanisms underlying dislocation annihilation and the growth of low defect II-VI materials on severely lattice-mismatched substrates. In addition, substantial contributions were made by Dr. Karl Hobart at the Naval Research Laboratory who identified the key fabrication steps and performed all of the wafer-bonding, etching, and substrate removal procedures required to produce the ultra-thin Si(211)-on-Si(100) layers that were subsequently analyzed at HRL and UCSB. Thin InGaAs-on-GaAs "compliant" substrates were supplied by Dr. T. Lin (University of Houston and Applied Optoelectronics, Inc).

This report describes our investigations of compliant substrate behavior in the InGaAs-GaAs system and on heteroepitaxy of II-VI semiconductors on Si(211)-Si(100) layers. The results of the technical studies that addressed the two principal program objectives are presented in Section II. A summary of the technical progress as well as conclusions drawn from this work are presented in Section III. The period of performance for this program was October 15, 1998 to October 14, 2001, with a six-month program hold from July 14, 2000 to January 31, 2001. Dr. William Coblenz was the DARPA Program Manager, and Major Daniel Johnstone (USAF) was the Contract Monitor.

Section 2
RESULTS AND DISCUSSION

2.1 "TWIST-BONDED" COMPLIANT SUBSTRATES FOR III-V EPITAXY

Compliant substrates for the growth of III-V epitaxial films were investigated in this program for the heteroepitaxial growth of materials in the GaSb/InAs/AlSb family which have lattice constants near 6.1Å. This family of "6.1 Å" Sb-based materials has been shown to have significant advantages with regard to speed, flexibility in device design, and mitigation of unwanted defects compared to more conventional III-V materials and structures, and they are currently being investigated as the baseline materials in ultra-high-speed nanoelectronics programs. They are also finding widespread use in fabrication of very long wavelength IR detectors and mid-IR lasers. Although the utility of these materials is now well established, a suitable low-cost, robust substrate that is fully compatible with the 6.1Å device layers is not currently available. (GaSb is routinely used, but its high cost and small size make it an undesirable alternative in future applications of this technology). However, reports by Lo and co-workers at Cornell University several years ago, and by Lin and co-workers at the University of Houston suggested that very thin (<100 Å) layers of a III-V semiconductor appropriately bonded to a semiconductor support wafer could serve as a "compliant substrate" whose lattice spacing would conform to the lattice characteristics of the epitaxial film deposited upon it. They proposed that layer compliancy could be achieved through a process they referred to as "twist-bonding", and that such a twist-bonded compliant layer could potentially serve as a universal substrate for lattice-matching to a wide range of semiconductor materials. Based upon the remarkable possibilities offered by this claim, we conducted experimental and theoretical modeling studies in this program to test the compliant substrate concept and to evaluate the applicability of twist-bonded substrates for growth of high quality III-V device layers.

Initially, we planned to study GaAs-on-GaAs compliant substrates formed by the twist-bonding approach first demonstrated by Lo and co-workers. However subsequent reports from researchers at the University of Houston and at the Wright Air Force Research Laboratory suggested that better success might be achieved with thin InGaAs layers bonded to GaAs. Consequently, we made arrangements with Applied Optoelectronics, Inc. (AOI), a spin-off company affiliated with the University of Houston, to purchase a small quantity of their InGaAs-on-GaAs substrates. These substrates were examined using optical microscopy, atomic force microscopy (AFM), transmission electron microscopy (TEM), and by Auger spectroscopy depth profiling, and *in situ* experiments were conducted in the MBE chamber.

2.1.1 Surface and Structural Analysis of "Twist-Bonded" Substrates

The AOI process for producing InGaAs-on-GaAs compliant substrates begins with the twist-bonding of a wafer containing a thin (50-80Å) epitaxial film of InGaAs grown on InP to a bare GaAs "handle" wafer. After bonding, the InP substrate is completely removed by wet chemical etching, and the resulting GaAs/InGaAs sample is used as the substrate for MBE of mismatched epitaxy of other III-V layers. Upon examining samples of InGaAs-on-GaAs compliant substrates provided by AOI, it became clear that there are significant problems with de-lamination of the thin InGaAs layer from the GaAs substrate. Many samples contained only scattered remnants of the InGaAs film, making them totally unsuitable for epitaxial growth experiments. The AFM image in Figure 2.1 shows an example of the surface morphology and of a representative sample. Pieces of the bonded InGaAs film can be seen scattered over the GaAs substrate. Apparently in this case delamination occurred during etching of the sample to remove the InP substrate that was the original host for the InGaAs film.

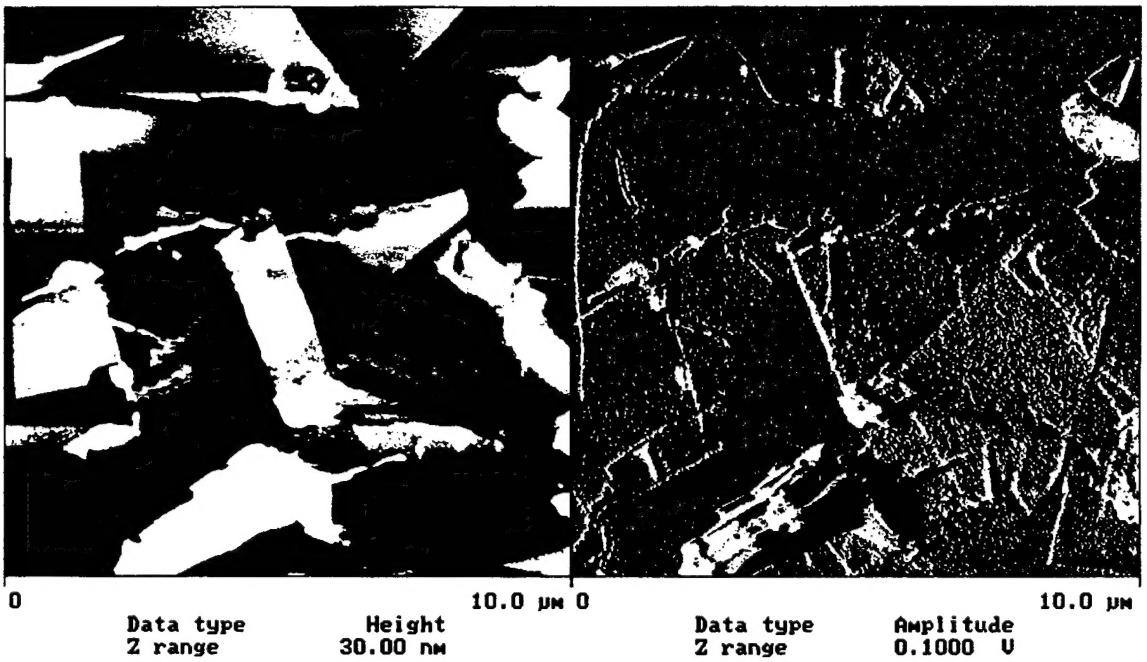


Figure 2.1. AFM images showing remnants of thin (80Å) InGaAs layer scattered around the GaAs surface as a result of delamination that occurred during etching. Left image is normal height-contrast mode; right image is derivative (edge-contrast) mode.

On a few of the samples we received from AOI, the InGaAs film survived the fabrication process. Figure 2.2 shows an Auger depth profile of such a specimen – the presence of a distinct InGaAs layer is clearly indicated. However, optical microscopy showed evidence of micro-cracking of the InGaAs layer, as seen in Figure 2.3, suggesting that some mechanical deformation of the layer had occurred during either the bonding or the separation (selective etching) process. In spite of this apparent problem, we placed a quarter-wafer specimen of this type of sample into the MBE growth chamber and subjected it to standard pre-growth thermal cleaning (i.e., oxide desorption by heating). High-energy electron diffraction (RHEED) analysis showed the presence of a layer whose principal crystallographic axes were rotated approximately 20° relative to those of the underlying GaAs substrate, consistent with the ≈ 20 degree twist angle used when bonding the InGaAs/InP wafer to the GaAs wafer at AOI. This "twisted" RHEED pattern persisted during heating, with fairly clear 1x1 streaks indicative of a planar specimen. However, upon reaching a substrate temperature of 560°C, the RHEED streaks degenerated into spots, indicating a 3-D deformation of the film had occurred. After cooling to 400°C in preparation for epitaxial growth of GaSb, the twisted RHEED pattern had completely disappeared, and only the substrate RHEED streaks were evident. The sample was examined after removal from the MBE chamber, and it was found that the InGaAs film had completely de-laminated from the substrate, making it impractical to continue with growth experiments. We point out that none of the InGaAs-on-GaAs samples received from AOI survived to the point where epitaxial growth could be initiated.

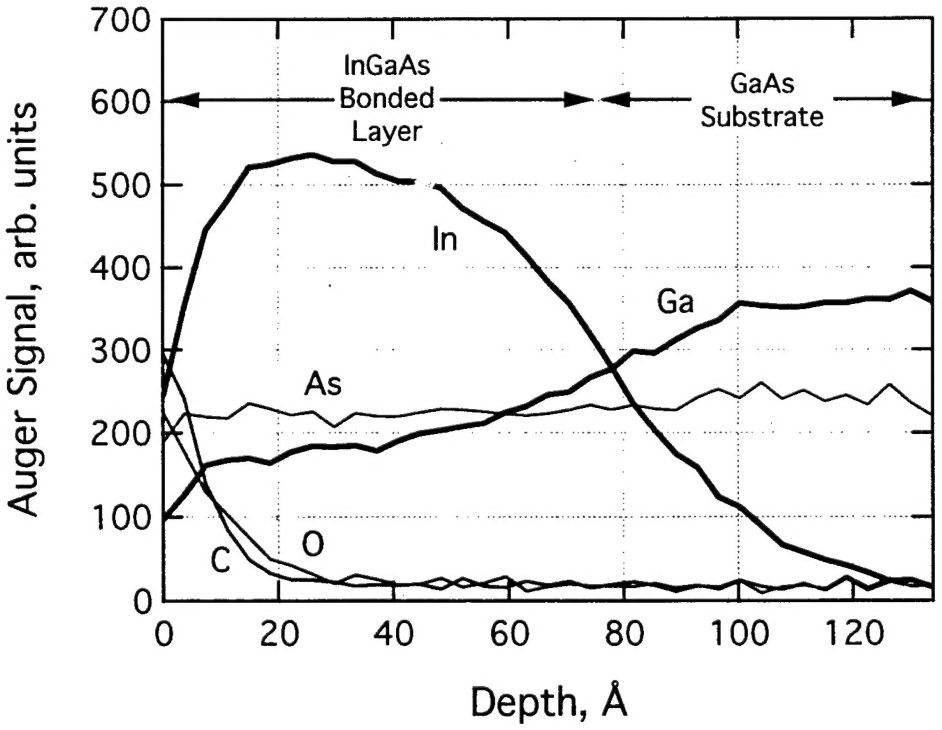


Figure 2.2. Auger depth profile of an InGaAs-on-GaAs compliant substrate specimen that survived the removal of the InP substrate without delamination of the InGaAs layer.

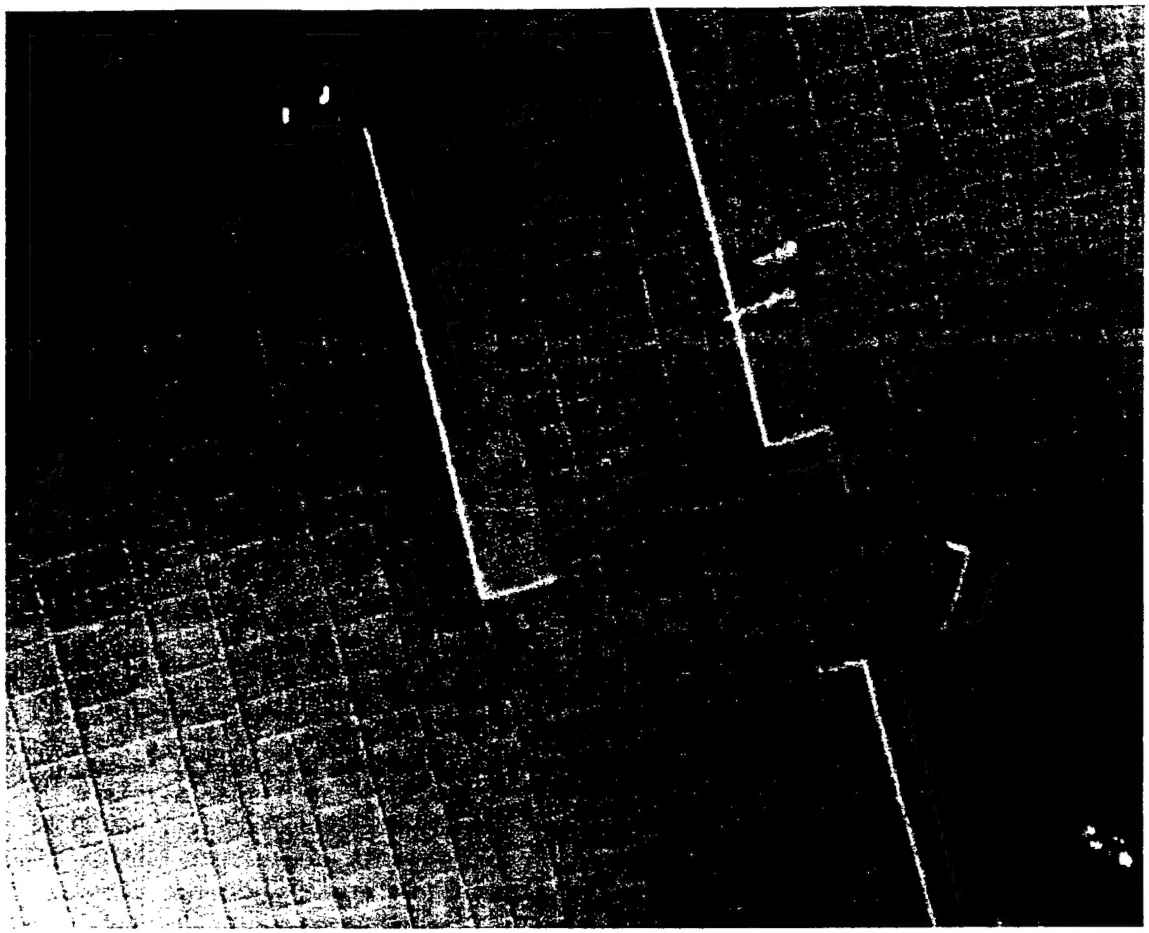


Figure 2.3. Optical (Nomarski) micrograph of specimen from Fig 2.2 showing mesoscale cracking of InGaAs layer bonded to GaAs. Image magnification is 1000x as printed.

Although we were unable to perform any actual growth experiments on InGaAs-on-GaAs compliant substrates prepared by AOI, they were able to provide a sample on which a complete laser structure had been grown in their laboratory. We performed TEM characterization of this sample to ascertain whether any direct evidence of compliancy could be observed. Lasers fabricated on other pieces of this particular sample had previously been tested by AOI investigators, and they interpreted the performance characteristics as implying that a high degree of defect (threading dislocation) reduction had occurred in these structures relative to companion samples grown on standard GaAs substrates. To test the hypothesis about threading dislocation reduction, we performed plan-view TEM analysis (see Figure 2.4). The TEM micrograph in Figure 2.4 shows that the threading dislocation density is at least 1.4×10^8 cm^{-2} in the AlSb layer adjacent to the compliant substrate (i.e., directly on top of the InGaAs "compliant layer"). This high density of dislocations is comparable to that which is obtained when a similar film is grown directly on standard GaAs, suggesting that no appreciable compliancy in fact occurred in the growth on a bonded InGaAs-on-GaAs "compliant" substrate.

Figure 2.4. Plan-view TEM micrograph of laser structure grown by AOI on a "compliant substrate" consisting of an 80Å InGaAs layer bonded to GaAs. In addition to threading dislocations, at the center of the image is a defect bundle probably comprising stacking faults together with a tangle of dislocations.

The results of the surface analysis studies conducted in this program have raised serious questions about the validity of the conclusions and interpretations made by Lin *et al.* concerning the existence of an InGaAs compliant interlayer. To examine the issue further and to provide the information needed to make a more unequivocal statement about 'compliant layer' behavior we conducted a series of *in situ* and *ex situ* spectroscopic ellipsometry measurements to test for the presence of the interlayer at various stages of processing. The results of those studies are summarized in the next section.

2.1.2 Spectroscopic Ellipsometry Analysis of InGaAs-on-GaAs Compliant Layers

Spectroscopic ellipsometry (SE) is a powerful analytical technique that is extraordinarily sensitive to the thickness and composition of thin layers comprising a multi-layer semiconductor, metal, or dielectric structure. The technique provides direct information about the change in the polarization state of light reflected from the surface of the sample. Since the polarization state depends upon the structural and compositional characteristics of the surface, the measured changes in the polarization state can be used to infer the static characteristics as well as changes in the surface material characteristics that accompany heating, layer deposition, etching, or other processing.

The reflection of polarized light from a sample is traditionally expressed by the ellipsometric equation: $\rho = R_p/R_s = \tan(\Psi)e^{i\Delta}$, where ρ is the complex reflectivity ratio, and R_p and R_s are the complex electric field coefficients for p- and s-polarized light, respectively. Ψ and Δ are the "ellipsometric parameters" that represent the intensity ratio of p-polarized to s- polarized reflected light and the phase difference between the two polarizations. By conducting measurements over an extended wavelength range, detailed information can be extracted about the structural and compositional properties of surface and near-surface layers and the time-dependent changes in those properties during MBE growth experiments.

A 228-wavelength SE system developed and manufactured by J.A. Woollam, Co. Inc. was used in the experiments reported here. The system includes a complete capability for multiple wavelength data acquisition, and a powerful integrated software package for real-time analysis of *ex situ* data acquired 'on the bench' and *in situ* data obtained in the MBE system during growth. In the SE measurement Ψ and Δ pairs are acquired at each wavelength. The experimental data are then compared with predictions derived from a customized model that represents our best approximation to the real structure. Each layer in the model is characterized by a set of optical dielectric functions. By adjusting the model parameters (e.g., thickness, composition of a specific layer or set of layers), to minimize computed error between the model predictions and experimental data it is possible to obtain a "best fit" that most closely represents the real properties of the sample. In this section we will present predictions from the optical models, and we will present comparisons with the results obtained by fitting the model predictions to the actual experimental data. In addition we show the results of real-time, *in situ* monitoring of an InGaAs/GaAs compliant substrate during heating in the III-V MBE system.

To understand whether changes in the thickness of an InGaAs compliant layer could be readily detected using SE, we constructed an optical model that was our closest approximation to the structure of the "compliant" substrate. The model consists of a stacked structure consisting of an "effective medium approximation" (EMA) layer comprising GaAs and InGaAs dielectric

functions, an InGaAs compliant layer (CL), and an InGaAs-oxide layer on a GaAs substrate (see Figure 2.5).

InGaAs-oxide 15Å
InGaAs (CL) *vary thickness*
EMA (GaAs /InGaAs) 250Å
GaAs (substrate)

Figure 2.5. Optical/structural model for determining the sensitivity of psi and delta to variations in the thickness of the InGaAs compliant layer (CL).

The dielectric functions for each layer were obtained from an existing library of room temperature optical constants. The initial values for all parameters were determined by closest fit to experimental data. Those parameters were then held at fixed values and the thickness of the InGaAs compliant layer was varied from 0 to 100Å in increments of 10 Å. The effects of changes in the InGaAs compliant layer thickness on the psi and delta spectra are shown in Figure 2.6. The modeling results show a strong sensitivity of psi and delta to changes in the thickness of the thin InGaAs layer, and we were therefore confident that SE data would be able to unambiguously reveal the existence of a thin InGaAs layer if it was present in the structure.

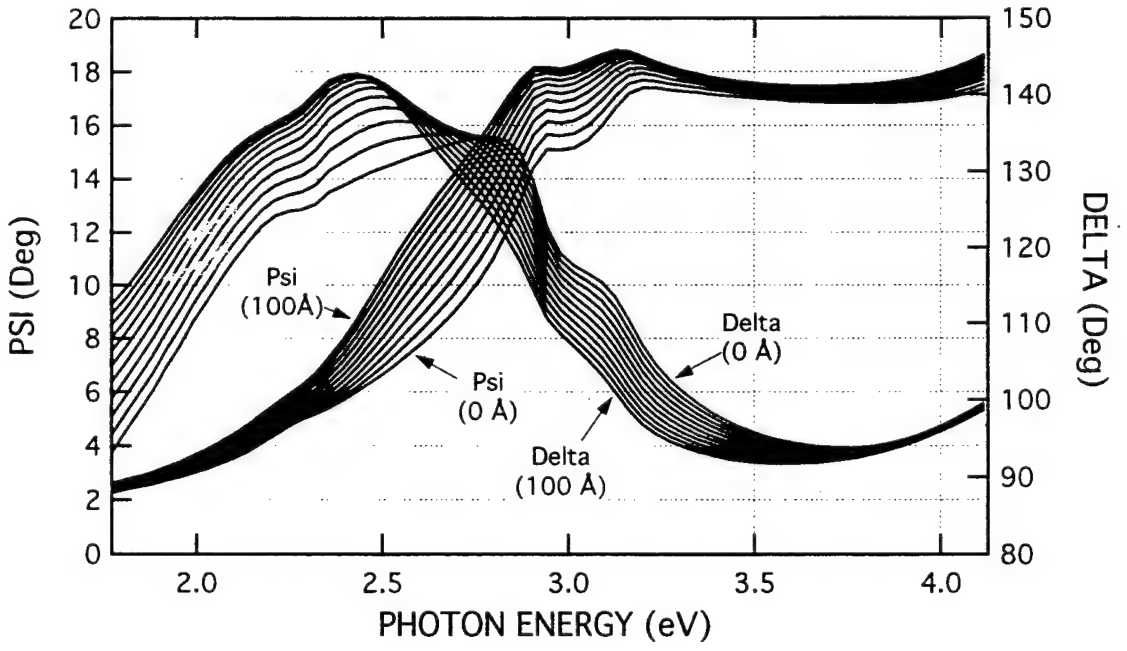


Figure 2.6. Sensitivity of psi (red) and delta (blue) to variations in the InGaAs CL layer thickness (derived from model shown in Figure 2.5). The annotation identifies psi and delta curves for InGaAs layers 0 and 100 Å thick.

Experimental SE data and the model fits to the experimental results are shown in Figure 2.7 for an InGaAs/GaAs sample provided by AOI. There is excellent agreement between the experimental data (red and blue solid lines) and the model results (dashed lines). This strongly suggest that a thin InGaAs layer *was present* on this particular sample and that the spatial extent of the layer is sufficiently large to permit a meaningful SE measurement (i.e., the layer didn't break-up into island structures that would have produced a degraded data fit). In this case, the thickness of the InGaAs layer that is inferred from the SE model is 58Å. We point out that when we compared the experimental data to a model containing an InGaAs layer with zero thickness, a poor fit to the data was obtained, lending further credence to the conclusion that an InGaAs layer did indeed exist on this sample.

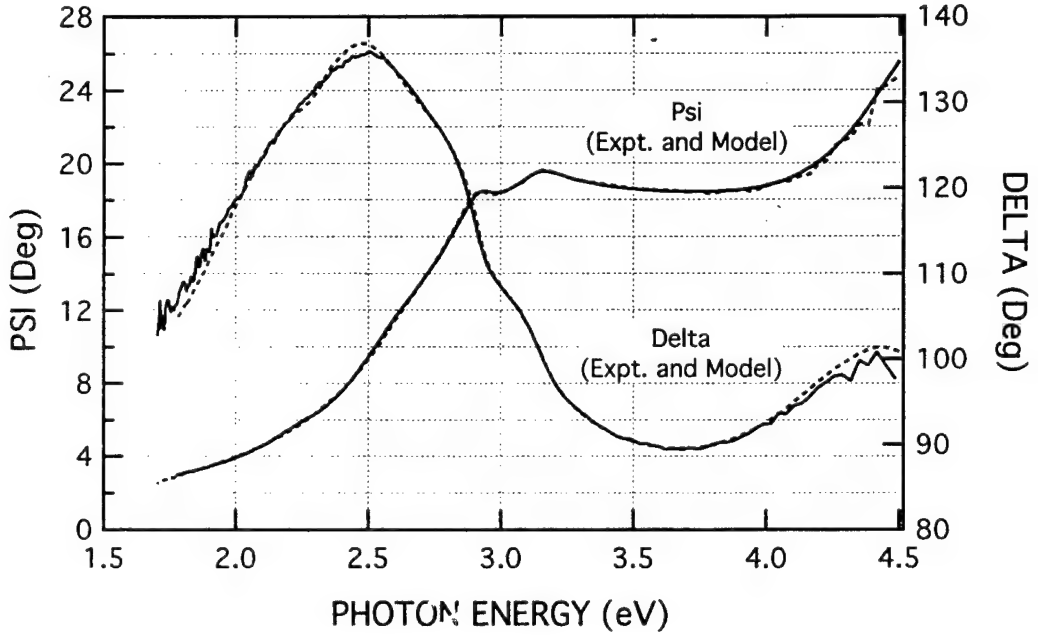


Figure 2.7. Experimental (solid lines) and model SE data (dashed lines) for an InGaAs/GaAs "compliant" substrate sample measured *ex situ* in air. Excellent agreement between experiment and model results suggests 58 Å thick InGaAs layer is present.

To investigate whether the type of InGaAs/GaAs sample described above could be used as a substrate for epitaxial growth of an Sb-based semiconductor film we inserted samples having initial *ex situ* SE signatures similar to those shown in Figure 2.7 into the III-V MBE system for growth experiments. The VG V-80H MBE system is equipped with *in situ* SE, absorption edge spectroscopy for substrate temperature measurement, and reflection high-energy electron diffraction (RHEED) for surface structure determination. Before initiating growth experiments it was necessary to desorb the native oxide that exists on the surface of the thin InGaAs "compliant layer". Oxide desorption was performed by heating the substrate to greater than 550°C in the UHV system. During oxide desorption we monitored the condition of the substrate surface with both RHEED and SE. The RHEED data showed a rotation in the pattern of diffraction streaks;

however, the SE data show quite convincingly that the InGaAs layer was not retained on the surface. Rather, it appeared to detach or desorb from the substrate during heating.

Figure 2.8 shows the thickness of the InGaAs layer as a function of time during heating in the MBE system. In this example, the best initial fit to the SE data was obtained when we employed an "effective medium approximation" (EMA) layer comprising both GaAs and InGaAs (major fraction) sandwiched between the GaAs substrate and the InGaAs-oxide layer. Although not shown here, the fit to the psi and delta data in this sample *before* heating definitely indicated the presence of a thin InGaAs layer, fully consistent with the initial RHEED observations. However, as shown in Figure 2.8, the inferred thickness of the InGaAs-containing EMA layer drops precipitously during the initial stages of the heating cycle. In this experiment we also fit for substrate temperature, which is also shown in the figure to indicate the approximate temperature at which the InGaAs layer disappears.

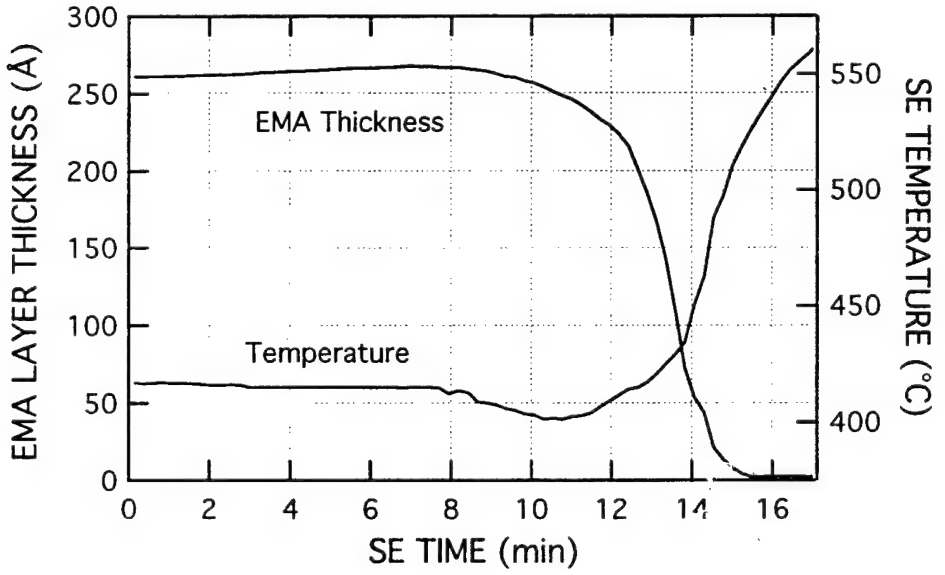


Figure 2.8. Thickness of InGaAs-containing EMA layer and substrate temperature inferred from *in situ* SE measurements of InGaAs/GaAs "compliant layer" sample as a function of time during heating in MBE system.

At the conclusion of the heating cycle, we re-examined the sample using the *in situ* SE system to confirm the conclusion that the InGaAs layer had indeed desorbed from the sample. We fit the experimental data using the same model that we used for the analysis during the oxide desorption experiment. (*Note*: the model shown in Figure 2.5 was not used for this analysis because the optical constants for the layers contained in that model only are appropriate at room temperature. For the *in situ* analysis a model containing temperature-dependent dielectric functions acquired in the appropriate temperature range was used). Figure 2.9 shows the experimental psi and delta data and the best fit obtainable using available dielectric function databases. The optical model that was used in the data fitting consisted of a GaAs substrate with temperature-dependent

optical constants, an InGaAs-GaAs EMA layer, and a surface layer that simulates surface roughness (an EMA layer containing a fixed fraction of voids).

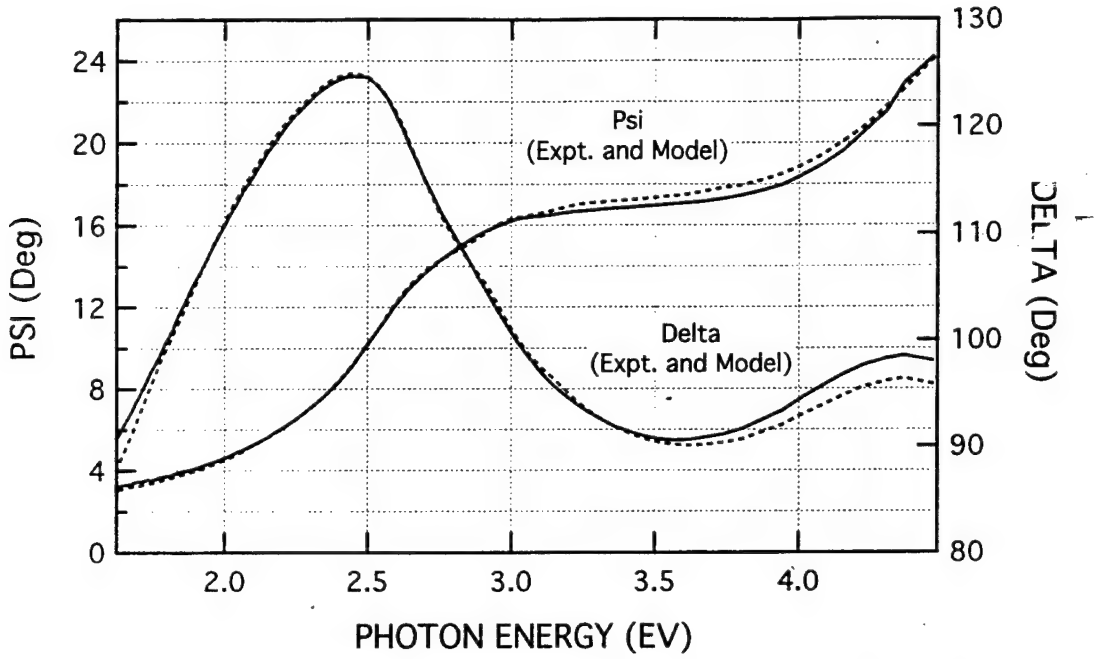


Figure 2.9. Psi and delta for InGaAs/GaAs sample after heating in MBE chamber. Measured data (solid lines) and model fits (dashed lines) using three-layer model with temperature dependent dielectric functions. Best fit to the experimental data obtained when InGaAs-GaAs EMA layer thickness is zero.

The best model fits to psi and delta (dashed lines in Figure 2.9) were obtained with a InGaAs-GaAs EMA layer thickness of zero and a dramatic increase in surface roughness (27Å) compared to 4.5Å obtained from fits to data acquired before heating the sample. This result supports the conclusions drawn from the desorption experiment and is consistent with the microscopy analysis presented in the previous section. Moreover, these results contradict the findings of Lin and co-workers who based their conclusions upon the observation of a rotation of diffraction features in the RHEED pattern which they interpreted in terms of a solid phase structural transformation in the twist-bonded InGaAs layer. RHEED measurements performed concurrently with the *in situ* SE measurements in our laboratory also revealed changes that could be interpreted in terms of a structural transformation in the InGaAs layer. However, given the compelling nature of the SE results and the results of post-growth microscopic characterization we strongly believe that the observed changes in the RHEED pattern arose solely from delamination/desorption of the thin twist-bonded InGaAs layer which then exposed the GaAs surface to the electron beam. The "rotated RHEED streaks" are then simply due the difference in the RHEED pattern from the InGaAs layer before delamination and the pattern obtained subsequently from a GaAs surface containing isolated patches of InGaAs.

In view of our inability to obtain usable III-V compliant substrates made by the "twist-bonding" method, the negative results with respect to dislocation density on layers reported by AOI to be "compliant", and the lack of SE data supporting the existence of a "compliant layer", we examined more closely the experimental evidence from the literature on compliant substrates for evidence of low threading dislocation density resulting from compliancy. Remarkably, it appears that in all cases, only cross-sectional TEM analysis was performed, making it impossible to derive meaningful threading dislocation densities (plan-view TEM is essential for this purpose). Unfortunately, the original samples upon which the original reports of compliancy by Professor Lo and co-workers at Cornell were based, are no longer available, making it impossible to directly check those results. For reasons discussed in Section 2.3, it presently seems unlikely that the twist-bonding approach will actually lead to significant threading dislocation reduction, especially in cases of large (>2%) lattice mismatch, where epitaxy proceeds via island formation and coalescence. There may be interesting side effects of growth on a twist-bonded thin layer, such as improved layer morphology as reported by some authors, but a direct, controllable and reproducible reduction of threading dislocation density to low levels seems unlikely.

2.2 DISLOCATION REDUCTION IN GROWTH OF II-VI MATERIALS ON SILICON

The second topic addressed in this program involves the development of research strategies and experimental approaches for growth of HgCdTe and other II-VI materials on Si(100), and the development of a better understanding of dislocation formation in the heteroepitaxy of Group II-VI materials on Group IV substrates. As stated previously, an important potential application of this particular material combination involves the growth of HgCdTe IR detector structures with low defect densities on Si(100) substrates. This is a critical step in realizing the goal of monolithic integration of IR detector and read-out functions in a single wafer.

2.2.1 Formation of Si(211) Layers on Si(100) Substrates for II-VI Epitaxy

It is possible to grow HgCdTe detector layers on <211>-oriented Si substrates, but growth directly on Si(100) substrates is not possible without introducing an excessive concentration of defects or compromising the ability to extrinsically dope the HgCdTe epitaxial layer. To overcome this incompatibility, in collaboration with NRL and UCSB, we investigated a wafer-bonding approach to create a composite substrate comprising an ultra- thin Si(211) layer on a Si(100) substrate. The successful implementation of this thin film technology may be the key enabler for direct integration of HgCdTe IR detectors grown on Si(211) with readout electronics embedded in the Si(100) substrate. The approach for formation of the thin "compliant" substrate structure is depicted in Figure 2.10.

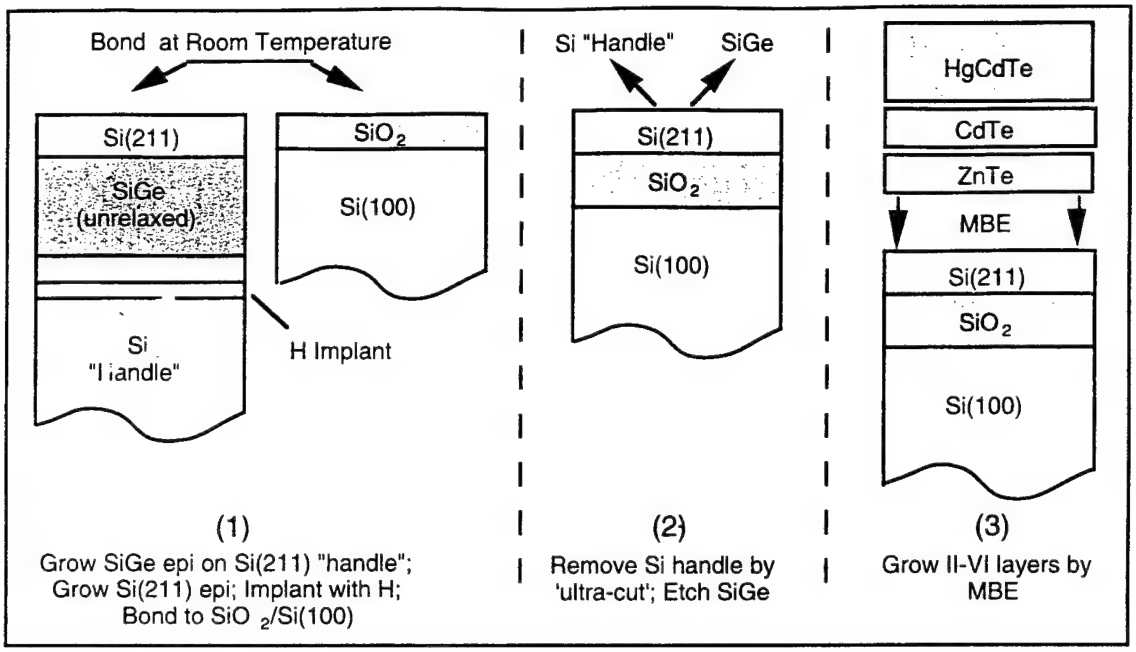


Figure 2.10. Procedure for wafer bonding of Si(211) epitaxial layer to Si(100) substrate for growth of II-VI layers.

In this approach, a SiGe epitaxial layer is grown on a Si(211) "handle" wafer by MBE (Step 1 in Figure 2.10). The thickness of the SiGe (~300Å) is less than the threshold for strain relaxation to ensure lattice-matching with the subsequently grown 50-70Å thick Si(211) layer. Hydrogen is ion-implanted to form a buried layer ~5000Å beneath the surface. The wafer containing the thin Si(211) layer is then bonded at room temperature to a second Si wafer that contains a 2300 Å-thick thermally grown oxide layer. This bond is typically strengthened by heating to approximately 200°C in nitrogen. At this point, the bonded wafer pair is examined by IR transmission measurements to evaluate the success of the bond with respect to uniformity, trapped voids, etc. Step 2 involves heating the bonded wafer pair to 450°C in nitrogen to cause ion-induced splitting at the position of the implanted hydrogen layer, resulting in delamination of the Si handle wafer. The excess remaining Si and the SiGe layer are then removed by wet etching. This exposes the Si(211) surface, which serves as the substrate for subsequent growth of ZnTe/CdTe/HgCdTe layers in the II-VI MBE system.

Considerable effort was devoted in this program to the development, optimization, and implementation of the processes in Steps (1) and (2) in Figure 2.10. Based on initial trials at NRL and qualification of commercial vendors to perform the initial steps of the process, we defined a lot of 75 Si(211) wafers for the initial batch, and sent out 60 of these to the vendor for processing. The remaining wafers were retained for future tests, and at each stage of the process we retained a fraction of the wafers as well for diagnostic measurements and process tracking. Wafers were sent to Lawrence Semiconductor for the SiGe and Si epitaxy, then to Implant

Sciences for the H ion-implantation to complete the "handle" wafer structure. The completed Si(211) "handle wafers" were then sent to BCO Technologies for bonding to oxidized Si(100) wafers which they supplied.

Upon receiving bonded wafer pairs from BCO, we performed several types of tests to determine whether it was appropriate to continue the process. Bonded pairs were examined using an IR camera, then subjected to heating to cause ion-splitting, and then re-examined. Unfortunately, the splitting was successful on only a small fraction of the wafers bonded at BCO. Some pairs actually split prematurely, at a low temperature. The majority of the wafer pairs showed non-uniform bonding in IR, which along with the other tests, indicated that the bond was too weak to stand up to the subsequent 450°C anneal required for ion splitting.

Extensive tests were performed to determine possible causes for the weak bonding observed. We concluded that BCO had probably not properly cleaned the two wafers ("handle" wafer and "device" wafer) prior to bonding, leaving trapped organic contaminants that volatilize during the splitting anneal, forming carbon dioxide bubbles that result in bond failure. This hypothesis was confirmed by using some of the wafers that we had set aside and had not sent to BCO for bonding. Karl Hobart (at NRL) applied his state-of-the-art cleaning process to the set-aside wafer pairs, and then bonded them at room temperature. This resulted in strongly bonded wafer pairs that successfully survived the subsequent ion-splitting anneal. There was still a small incidence of trapped "voids" at the bond interface, but several wafers were produced that contain large areas of uniform bonding. The best wafers were then etched to remove the Si that remains after ion-splitting, leaving only the SiGe layer intact, protecting the underlying thin Si(211) layer.

2.2.2 *Ex Situ* Characterization of Si(211) "Compliant" Substrates

Six four-inch wafers containing 50-100 Å-thick "compliant" Si(211) layers on Si(100) substrates were successfully prepared at NRL and delivered to HRL Laboratories for testing and MBE growth experiments. Figure 2.11 is a schematic cross-section of the test samples (the details of the sample preparation procedure are given in Figure 2.10).

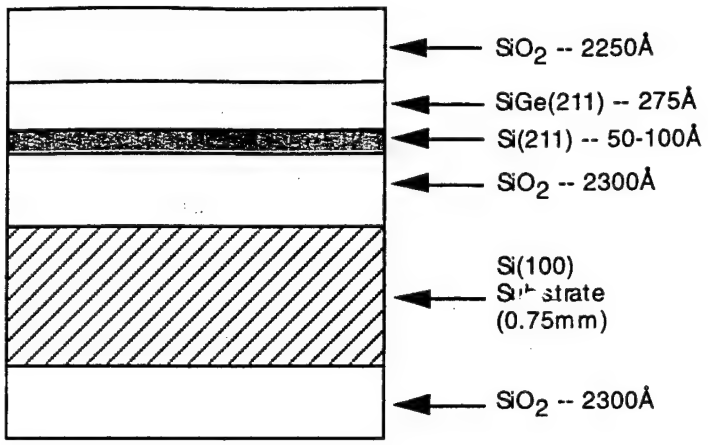


Figure 2.11. Cross-section of Si "compliant" substrate prepared at NRL and delivered to HRL Laboratories for II-VI layer growth.

The thin Si(211) "compliant" layer is protected by a SiGe (etch-stop) layer and an SiO_2 cover layer to protect the compliant layer during handling. These layers were removed by wet chemical etching before the II-VI MBE growth experiments were performed. A photograph of one of the four-inch test wafers is shown in Figure 2.12. In accordance with the contract requirements of this program, three 4" diameter "compliant" substrate wafers and six 1.5 cm x 1.5 cm test pieces weredelivered to Dr. Kurt Eyink, Wright Air Force Research Laboratory, for analysis and testing in his laboratory.

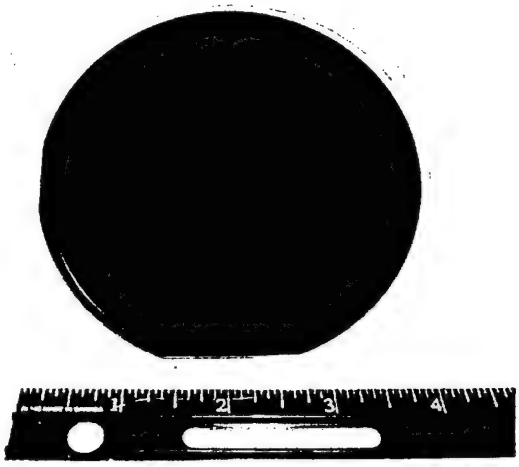


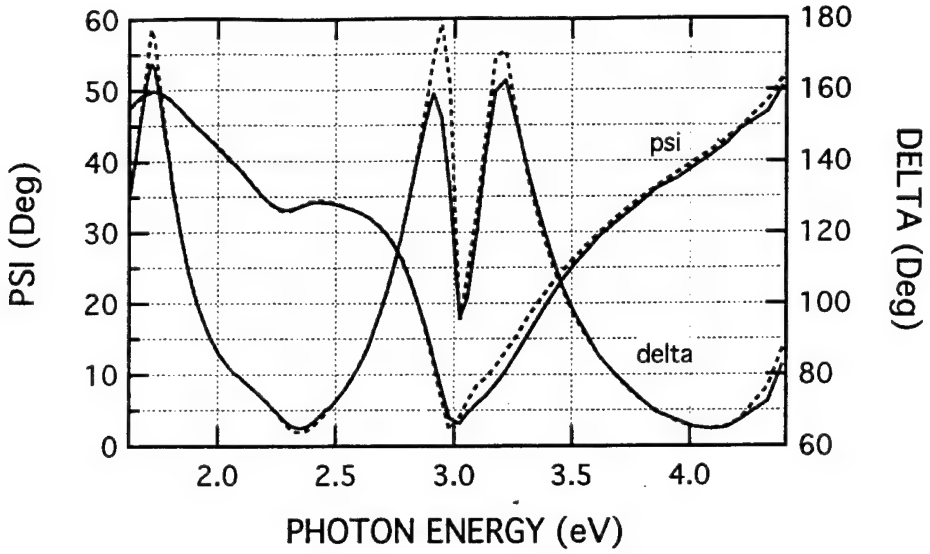
Figure 2.12 Photograph of 4-inch dia. "compliant substrate" wafer with cross-sectional structure shown in Figure 2.11. Wafer bonding to produce embedded thin Si(211) "compliant" layer performed at NRL.

The cleaning and etching steps that we employed for preparation of the samples for insertion into the MBE system are given in Table 2.1. This procedure resulted in exposure of the thin Si(211) layer with surface dangling bonds terminated by H atoms. The hydrogen was desorbed prior to II-VI epitaxy by heating in the MBE system.

Table 2.1. Procedure For "Compliant Substrate" Cleaning and Cap Layer Removal

3	RCA (SC-1) wafer clean.
4	Dice wafer into 1.5 x 1.5 cm pieces for mounting in the MBE system
5	D.I. rinse.
6	UV/ozone exposure—2 min (optional step—to remove any carbon-containing material that may have been present on the backside of the sample due to prolonged storage).
7	H_2O: HF (10:1) dip – 6 min, to remove thick oxide from front and back.
8	D.I. rinse.
9	Peracetic acid: HF (5:1) dip – 25 sec, to remove SiGe from the Si(211) "compliant" layer
10	D.I. rinse.
11	H_2O: HF (10:1) dip – 10 sec, to remove native oxide and terminate surface Si dangling bonds with hydrogen.

Prior to conducting experiments in the MBE growth system, we performed a series of *ex situ* spectroscopic ellipsometry studies on test pieces cut from the four-inch wafers. The objectives of the *ex situ* analyses were to evaluate the success of the wet chemical etching procedures for removing the oxide and SiGe cover layers, and to examine the quality and structural stability of the thin Si(211) layer at each step in the process.. The SE measurements were performed before and after each step in the sample preparation process, and the experimental data were compared with an optical model comprising dielectric functions for each of the layers in the structure. The model parameters (layer thickness, Si_xGe_{1-x} composition) were iteratively varied to minimize the difference between the experimental results and model predictions. An example of SE data (psi and delta) for one of the wafers after megasonic RCA surface cleaning, but prior to oxide and SiGe layer removal is given in Figure 2.13. The red solid and dashed lines are the experimental data and fits for psi, the blue solid and dashed lines show the corresponding experimental and model fits for delta. The thicknesses of the individual derived from the SE fitting procedure are also given in Figure 2.13.



SiO_2	1685 Å
SiGe (x=.786)	275 Å
Si(211)	112 Å
SiO_2	2298 Å
Si(100)	Substrate

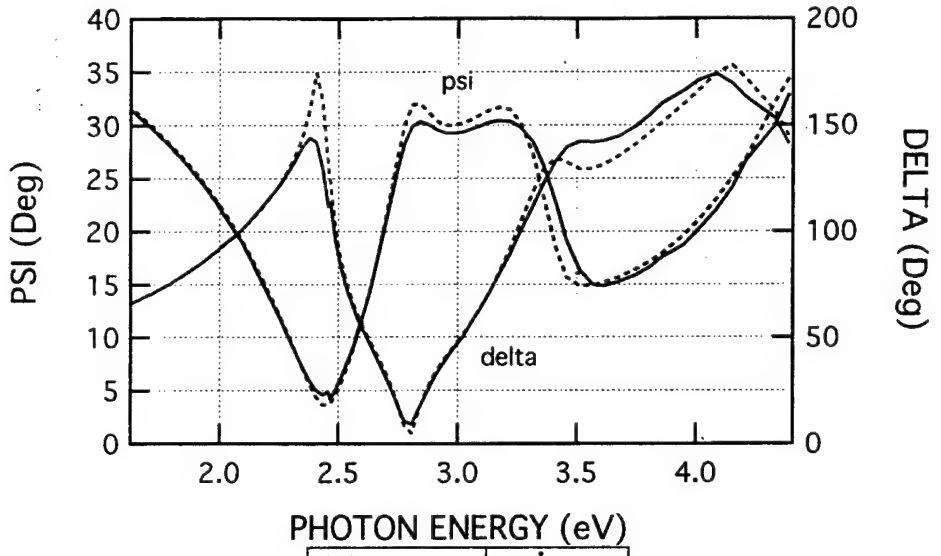
Figure 2.13. Experimental SE data (solid lines) and model fits (dashed lines) for "compliant substrate" sample after megasonic RCA surface clean. Table gives layer thicknesses derived from the model fit to the experimental data.

We point out that the accuracy of the SE analysis for such a complex structure depends upon the validity of the optical model and on the accuracy of the dielectric function databases used in the data fitting process. In this case, we used databases that were available in the dielectric function library supplied by J.A. Woollam Co. (The library is a compilation of optical constants for semiconductors, metals and dielectrics acquired from various sources). The good agreement between the experimental data and the model fits in Figure 2.13 indicate that the optical model is an acceptable representation of the physical state of the sample and that the dielectric functions are appropriate for this analysis. The six test wafers were analyzed in the same way. Table 2.2 gives the layer thicknesses derived from the SE data obtained for the six samples.

Table 2.2. Summary of SE-derived layer thicknesses for six Si "compliant layer" test wafers (composite structure shown in Figure 2.11).

Sample #	1	2	3	4	5	6
SiO_2	1685 Å	1711 Å	1629 Å	1482 Å	11169 Å	1574 Å
SiGe	275 Å	299 Å	278 Å	286 Å	278 Å	275 Å
Si(211)	112 Å	104 Å	99 Å	107 Å	96 Å	109 Å
SiO_2	2298 Å	2262 Å	2285 Å	2287 Å	2299 Å	2274 Å
Si(100)	Substrate	Substrate	Substrate	Substrate	Substrate	Substrate

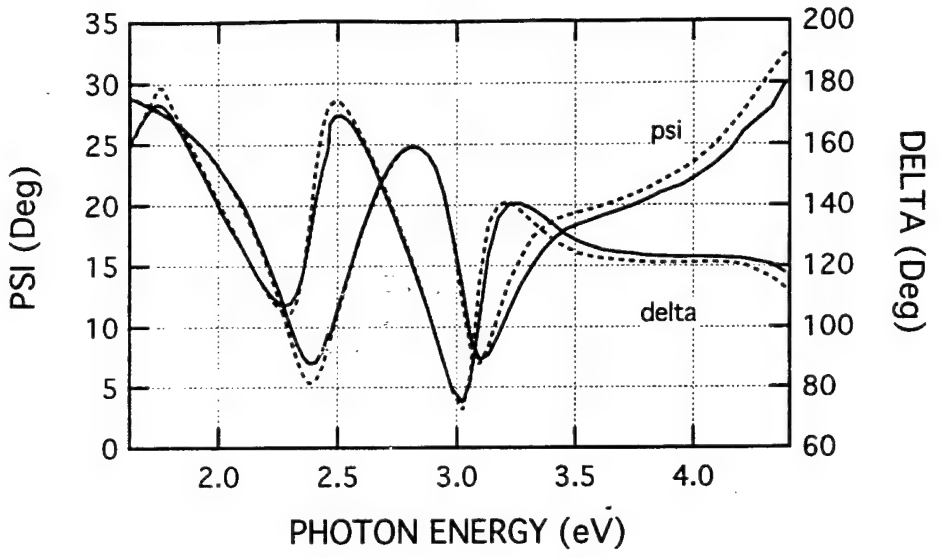
The *ex situ* SE data and derived layer thicknesses for the Si "compliant layer" sample after removal of the SiO_2 cap layer by etching in 10:1 H_20:HF solution for 6 minutes and are shown in Figure 2.14.



SiO_2	10 Å
SiGe (x=.786)	267 Å
Si(211)	115 Å
SiO_2	2305 Å
Si(100)	Substrate

Figure 2.14. Experimental SE data (solid lines) and model fits (dashed lines) for "compliant substrate" sample after removal of the thick SiO_2 capping layer. Table gives layer thicknesses derived from the model fit.

There is a significant difference in the psi and delta data and the results of the model fit after etching of the oxide layer (compare with Figure 2.13). The thin (10Å) oxide layer remaining after etching is the residual native oxide formed by air exposure. Removal of the SiGe etch-stop and cap layer was accomplished using a 5:1 peracetic acid:HF solution. This etching solution, recommended by Karl Hobart (NRL), works very well for selective removal of SiGe from the thin Si(211) layer. The *ex situ* SE data obtained on the sample after removal of the SiGe layer are shown in Figure 2.15.



SiO_2	1.3 Å
Si(211)	58 Å
SiO_2	2320 Å
Si(100)	Substrate

Figure 2.15. Experimental SE data (solid lines) and model fits (dashed lines) for "compliant substrate" sample after removal of SiGe layer to expose the thin Si(211) layer. Table gives layer thicknesses derived from the model fit to the experimental data.

After removal of the SiGe, the thickness of the Si(211) layer derived from the SE model fits decreases from about 110 Å to 58 Å. At this time we cannot definitively state whether the Si(211) layer thickness has actually decreased upon exposure to the peracetic acid/HF etching solution or whether the difference results from the SE fitting process. Since the minimization routine varies all of the layer thicknesses to determine the lowest mean squared error (MSE) between the experiment and the model, it is possible that the greater thickness derived for the layer embedded beneath an oxide and a SiGe cap may simply be due to the variability of the fitting routine. To further investigate the possible cause of this discrepancy we performed a series of SE model simulations in which we held all fitting parameters (layer thicknesses and SiGe composition) constant while the thickness of the Si(211) layer was varied from 40-100 Å in 10Å increments. We compared the results of the model simulations for three different structures: 1) the full composite structure (Figure 2.11) containing the Si(211) layer with SiGe and SiO_2 overlayers; 2) the same structure with the SiO_2 layer removed, and 3) the structure with both the SiGe and the SiO_2 layers removed (Si(211) surface exposed. In this way, it is possible to assess the sensitivity of the SE data to changes in the thickness of the Si(211) layer for the different structures and to thereby determine which structure would most likely produce the most physically reasonable value for the Si(211) compliant layer thickness.

Results of model simulations for the three different sample structures described above are presented in Figures 2.16, 2.17 and 2.18. It is apparent that the sensitivity to variation in the thickness of the Si(211) "compliant" layer becomes progressively greater as overlayers are removed from the Si(211) surface. In the case of the full composite structure (Figure 2.16), there is minimal sensitivity to the thickness of the Si(211) layer, whereas there is a marked dependence of the psi and delta data to Si(211) thickness in the structure where the Si(211) layer is exposed (Figure 2.18). Based upon this strong sensitivity to layer thickness we conclude that the latter optical model gives the best representation of the Si(211) "compliant" layer thickness and that the layer thickness is approximately 58Å (Figure 2.15). (This, of course, still does not rule out the possibility that the layer thickness may have decreased upon exposure of the Si(211) to the peracetic acid/HF etching solution).

The full composite structure and associated thicknesses used for the simulations in Figure 2.16 are shown below. Figure 2.17 shows the results when the SiO_2 layer is removed, and Figure 2.18 gives the result when both the SiO_2 and SiGe layers are removed, exposing the "bare" Si(211) "compliant" layer.

SiO_2	1574 Å
SiGe (x=.786)	275 Å
Si(211)	Vary (40-100 Å)
SiO_2	2274 Å
Si(100)	Substrate

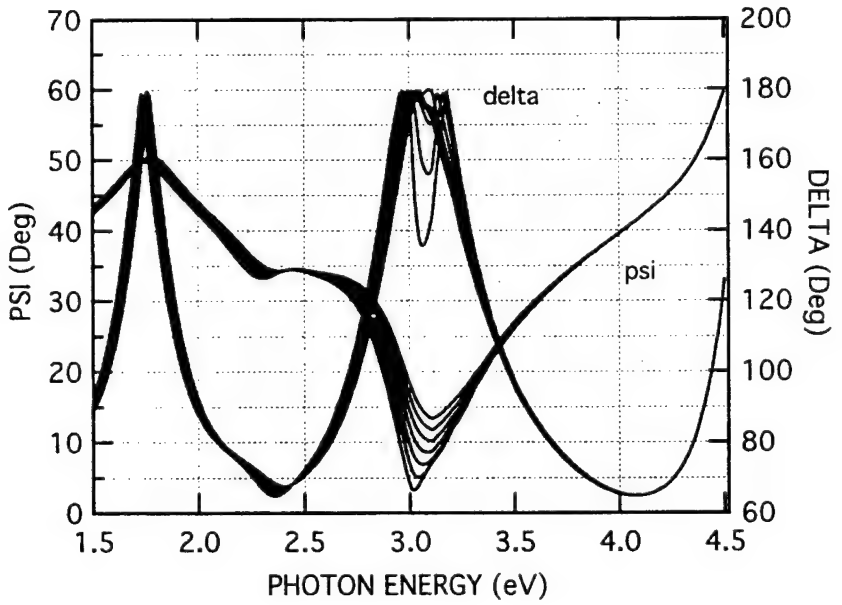


Figure 2.16. Simulated SE data for full composite structure (incl. SiO_2 and SiGe overlayers); Si(211) layer thickness varied from 40-100 Å in 10 Å increments. SE data show minimal sensitivity to changes in Si(211) layer thickness.

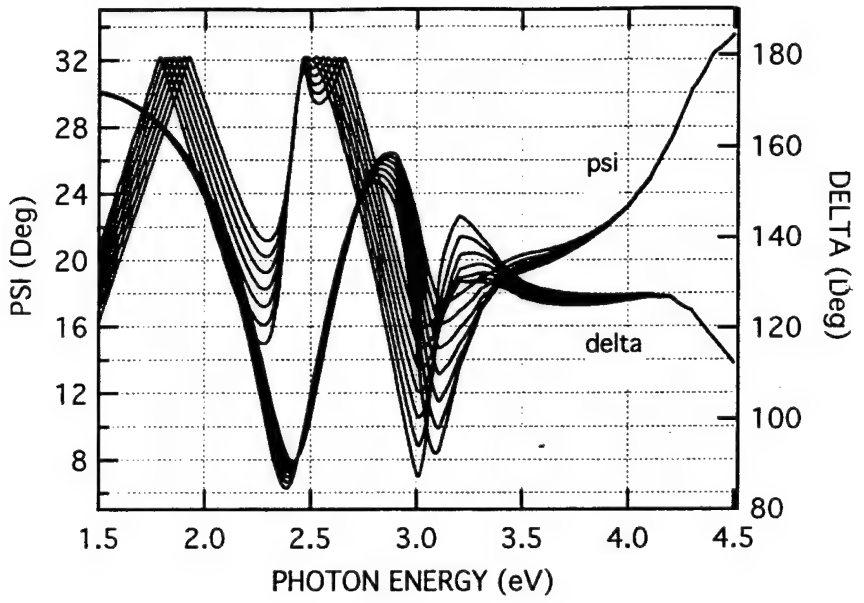


Figure 2.17. Simulated SE data for composite structure with SiGe overlayer only (no SiO_2 overlayer). Si(211) layer thickness varied from 40-100 Å in 10 Å increments. Moderate sensitivity to changes in Si(211) layer thickness.

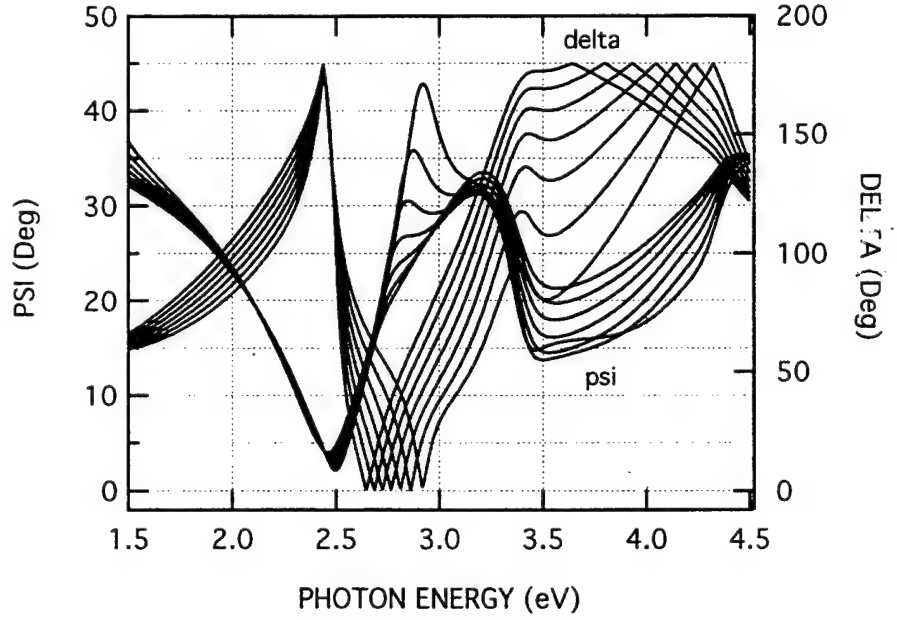


Figure 2.18. Simulated SE data for composite structure with no overlayers on Si(211). "Compliant" layer thickness varied from 40-100 Å in 10 Å increments. SE data show strong sensitivity to changes in Si(211) layer thickness.

The SE data presented in this section show how the values of the ellipsometric parameters, psi and delta, depend upon the structure and optical characteristics of the "compliant" layer samples.

Although these changes effectively illustrate the sensitivity of the SE technique to the multi-layer structures used in this study, the dielectric functions, ε_1 and ε_2, provide a "more physical" representation of how the materials in the composite structure respond to the applied electric field. Figure 2.19 shows dependence of ε_1 and ε_2 on photon energy for the simulation shown in Figure 2.18 in which the "compliant" Si(211) layer contains no overlayers and the thickness is varied from 40-100 Å. As is the case with the ellipsometric parameters plotted in Figure 2.18, the ε_1 and ε_2 data vary markedly with changes in the thickness of the Si(211) layer. We also point out that the dielectric function data also show minimal changes when the Si(211) layer thickness is varied in the composite structure (with SiO_2 and SiGe overlayers on the Si(211) "compliant" layer).

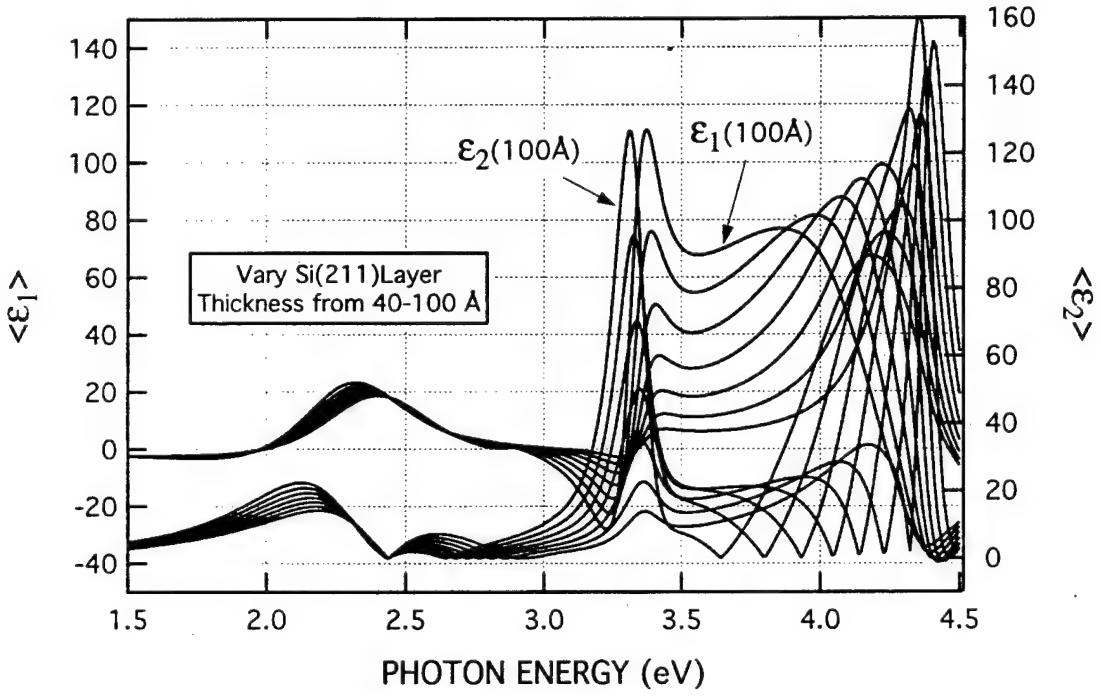


Figure 2.19. Dependence of the pseudo-dielectric functions, ε_1 and ε_2, on changes in Si(211) layer thickness in sample containing a thin Si(211) layer on an oxide-coated /Si(100) substrate (same as in previous figure). Si(211) layer thickness varied from 40-100 Å in 10 Å increments.

To conclude this section we present atomic force microscopy (AFM) data on the surface morphology of the thin Si(211) "compliant" layer present after etching away the SiO_2 and SiGe overlayers (see Figure 2.20). Prior to AFM analysis the Si(211) layer was treated with HF to terminate surface dangling bonds with hydrogen atoms. The data were obtained using a Quesant AFM system operating in the contact mode, and the AFM image was acquired near the center of the 1.5 cm square test sample. The x and y axes in Figure 2.20 span a 1000 nm range, and the z-axis spans a 24 nm range. The RMS roughness computed from the AFM data is 2.83 Å. This is comparable to the RMS roughness measured on a bulk Si reference sample..

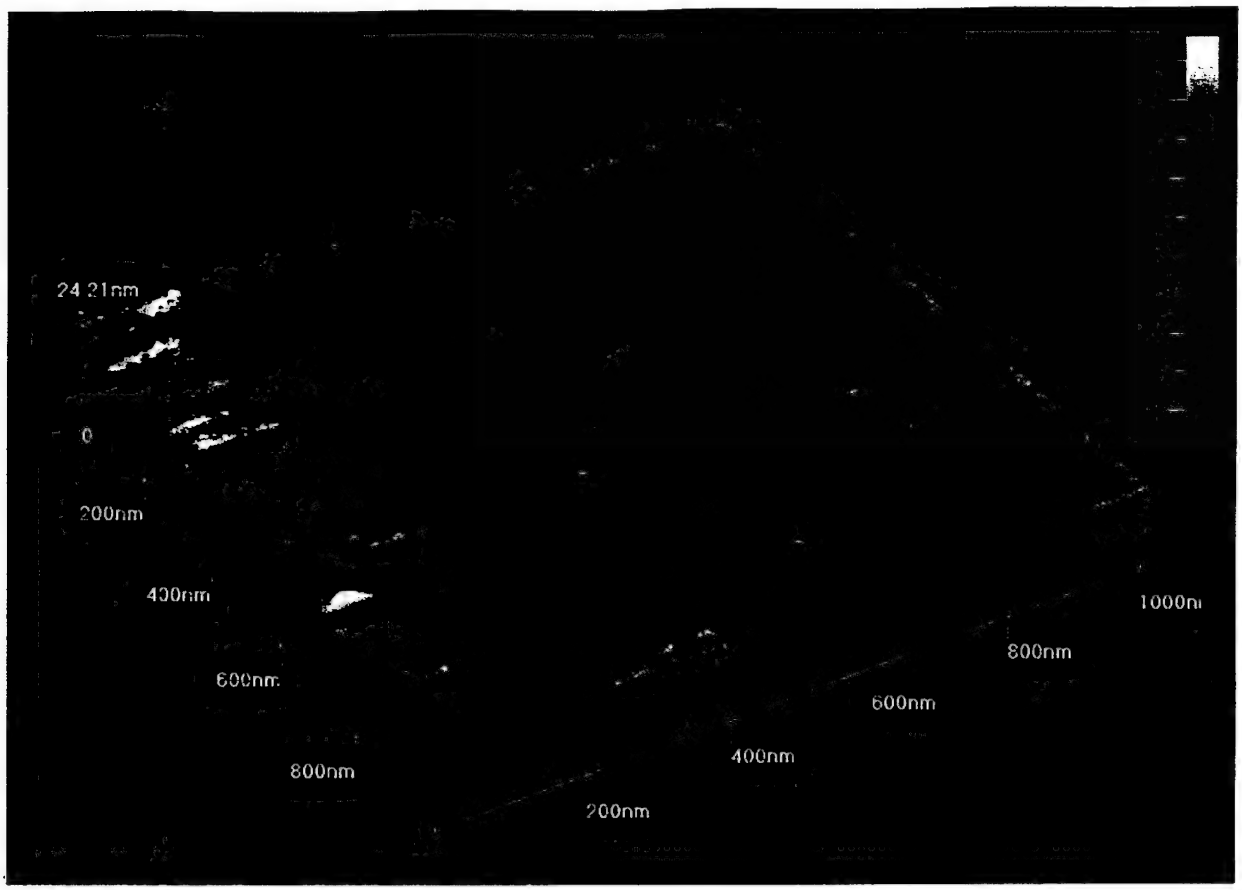


Figure 2.20 Atomic force microscopy image acquired on a 56Å thick Si(211) "compliant" layer with surface dangling bonds terminated by hydrogen (x and y scales: 0-1000 nm; z-scale: 0-24 nm; RMS roughness: 2.83 nm

2.2.3 MBE Growth and *In Situ* Characterization of II-VI layers On Si (211) "Compliant" and Bulk Substrates

The II-VI MBE growth experiments represented a significant component of the total technical effort in this program. There were four distinct, but related objectives in the MBE experiments.

- To determine whether the 58Å thick "compliant" Si(211) layer can withstand the pre-growth heating and H desorption steps without delaminating from the underlying substrate.
- To grow II-VI epi layers (ZnTe, CdTe, HgCdTe) on the thin "compliant" Si(211) substrates and to evaluate the defect and structural characteristics of the resulting layers.
- To compare the defect characteristics of II-VI layers grown on ultra-thin "compliant substrates with II-VI layers grown on bulk Si(211), "wafer-bonded" Si substrates with 2-5 μm-thick Si(211) layers, and "SIMOX" substrates with 1500-2000 Å thick Si(211) layers.

- To determine whether it is possible to nucleate single crystal HgCdTe layers directly on the thin Si(211) compliant layers and thereby obviate the need for intermediate buffer layers required for HgCdTe growth on conventional Si substrates.

The MBE growth experiments were conducted at HRL Laboratories using a customized VG80H MBE system schematically illustrated in Figure 2.21. The MBE system is equipped with *in situ* sensors for monitoring substrate temperature (absorption edge spectroscopy), epilayer composition (spectroscopic ellipsometry), surface crystallinity (reflection high-energy electron diffraction), and Cd effusion cell flux (atomic absorption). (For clarity, the latter two sensor systems are not shown in the figure). The absorption-edge spectroscopy system (NTM-1) is manufactured by CI systems, Inc. The *in situ* spectroscopic ellipsometer is a 228-channel rotating compensator system (M2000) manufactured by J. A. Woollam, Co., Inc. The incident light from the optical source and the light reflected from the sample are transmitted through low birefingence (Bomco) windows. Analysis of all SE data was performed using the WVASE/GrowthManager software package from J.A. Woollam Co.

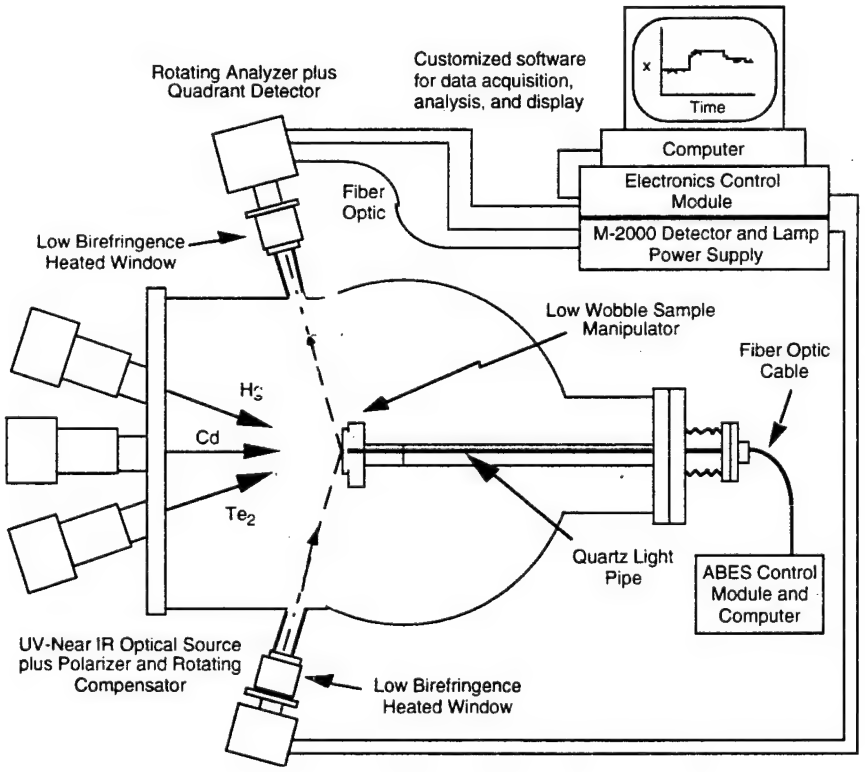


Figure 2.21. Schematic illustration of II-VI MBE system showing *in situ* spectroscopic ellipsometry and absorption edge spectroscopy sensors for real-time monitoring of layer composition and substrate temperature.

Four different types of samples were used in the MBE growth experiments: 1) Bulk Si(211) substrates, 2) "wafer-bonded substrates comprising a 2-5 μm-thick Si(211) layer bonded to an oxidized Si(100) wafer, 3) a "SIMOX" substrate comprising a 1500-2000 Å thick Si(211) layer separated from a bulk Si(211) substrate by a 1000 Å-thick, ion-implanted oxide layer, and 4) the "compliant" substrate comprising a 58 Å thick Si(211) layer separated from a Si(100) substrate by a 2300 Å-thick oxide layer. By using these samples it was possible to directly compare the dependence of the defect characteristics in the II-VI epilayers on the thickness of the Si(211) substrate (growth template). The four sample configurations are shown in Figure 2.22.

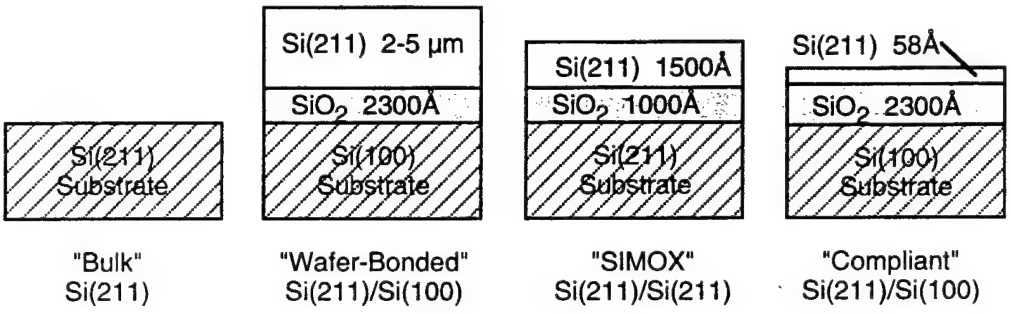


Figure 2.22. Cross-section of Si substrates used for the MBE growth experiments.

There is considerable experience at HRL on the growth of II-VI materials on Si substrates, and we have identified a "standard process" for obtaining II-VI layers with high structural quality. The first few growth runs in the II-VI growth campaign for this program were devoted to refining the growth conditions on bulk Si(211) substrates to provide a solid baseline for growth of II-VI layers on wafer-bonded, SIMOX, and "compliant" substrates. We used "free-mounted", radiantly heated 3-inch Si(211) substrates for the tune-up runs. The growth recipe involved thermal desorption of the adsorbed hydrogen, followed by deposition of a proprietary, thin surface passivation layer, deposition of a 1 μm-thick ZnTe buffer layer, and growth of an 8 μm-thick CdTe layer. The nominal target values for defect density (etch-pit density) and crystallographic quality (double-crystal, x-ray rocking curve) of the MBE-grown CdTe layers on bulk Si(211) are $2x10^6$ cm^{-2} and 100 arc-sec, respectively. Those values were obtained on the second growth run in the series, allowing the baseline growth conditions (substrate temperature, effusion cell fluxes) to be established for subsequent growth runs on "non-standard" substrates.

Nomarski interference contrast micrographs of the CdTe surface before and after defect etching (to reveal dislocations intersection the free surface) and x-ray double-crystal rocking curve (DCRC) data showing the crystallographic quality of the layer are shown in Figure 2.23. The etch-pit density is $2.2x10^6$ cm^{-2} and the DCRC peak for the single crystal layer has a FWHM of 90 arc-sec. These values are comparable to the best values that we have achieved in our laboratory for growth of CdTe on Si(211) and are remarkably good given the nearly 20% lattice mismatch between the CdTe epilayer and the underlying substrate.

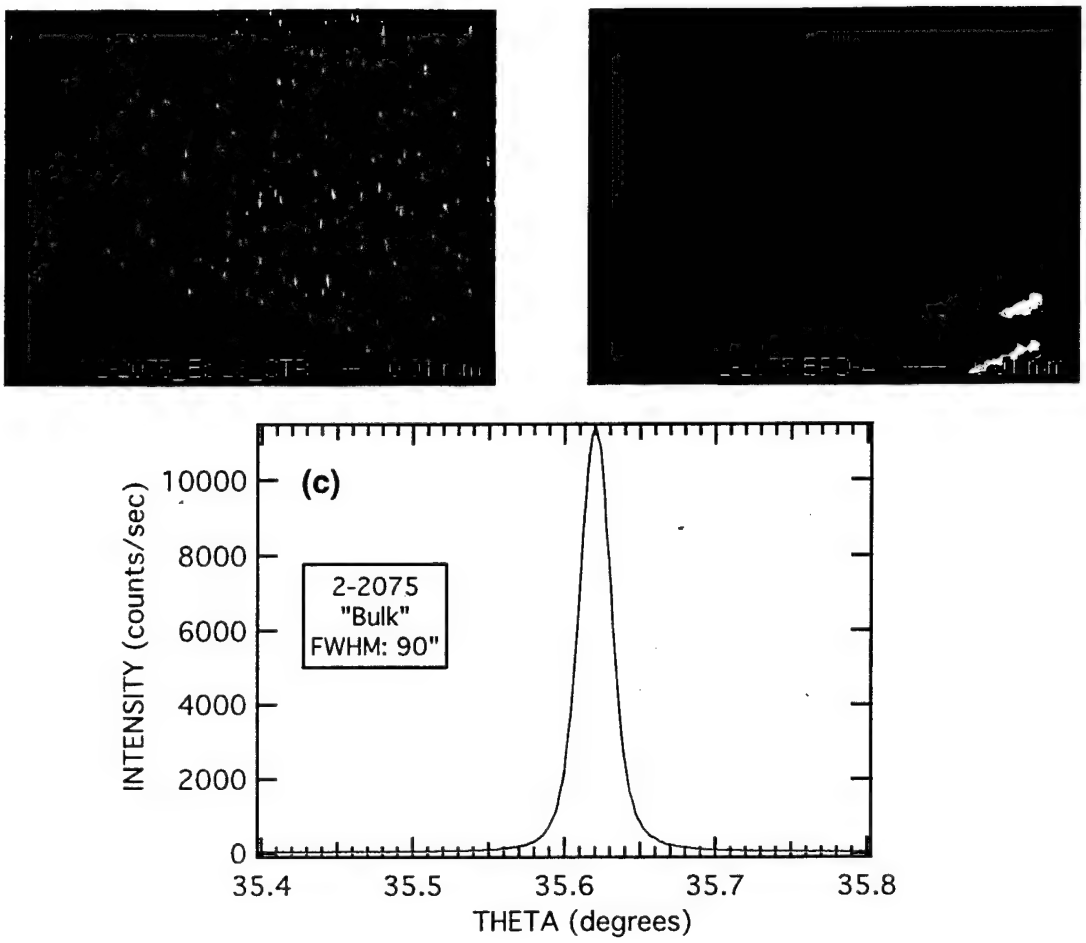


Figure 2.23. Surface morphology and structural quality of 8μm-thick CdTe layer grown on a bulk Si(211) substrate: (a) Nomarski micrograph of CdTe surface; (b) micrograph after defect etching to reveal surface dislocations (EPD: 2.2×10^6 cm^{-2}); (c) x-ray rocking curve (FWHM: 90 arc-sec).

The same growth conditions used for CdTe growth on 3-inch dia. Si(211) bulk substrates were used for growth of CdTe on the three-inch wafer-bonded Si(211)/oxide/Si(100) substrates and the SIMOX Si(211)/oxide/Si(100) substrates. In both cases, the results obtained for the structural quality and defect properties of the epitaxial CdTe layers on those substrates were comparable to the properties of layers grown on bulk Si(211) (see Table 2.3). This is an important result because it provides a straightforward pathway for growth of II-VI layers on Si(100) substrates, and it underscores the importance of wafer bonding as a potentially critical process component in the monolithic integration of high performance infrared detector structures with Si-based readout circuits.

Table 2.3. Summary of x-ray DCRC and EPD values for MBE-grown CdTe layers on "bulk" Si(211), "wafer-bonded" Si(211), "SIMOX" Si(211), and "compliant" Si(211) substrates.

Sample I.D.	Description	Si(211) Thickness	CdTe x–ray (DCRC)	CdTe x–ray (Θ-2Θ)	CdTe EPD
2075	CdTe/Bulk Si(211) 3" dia.	0.75 mm (Bulk	80"	Single	2.20E+06
2076	CdTe/"Wafer-Bonded" Si(211) 3" dia.	2 μm	87"	Single	1.90E+06
2077	CdTe/"SIMOX" Si(211) 3" dia.	1500 Å	90"	Single	2.10E+06
2079	CdTe/"Bulk"Si(211) 1.5x1.5 cm	0.75 mm (Bulk	93"	Single	2.20E+06
2081	CdTe/"Compliant" Si(211) 1.5x1.5 cm	55 Å	117"	Single	2.70E+06

Next, we conducted II-VI growth experiments using thin Si(211) compliant substrates. Prior to removal of the oxide and SiGe overlayers, the samples were "diced" into 1.5 cm square pieces. The test pieces were cleaned, etched, and surface-passivated using the procedure outlined in Table 2.1, and they were mounted on graphite holders that contained a hole, which permitted radiant heating of the substrate. Because this sample heating geometry was slightly different from the configuration used for the 3-in dia. wafers, we conducted a temperature calibration run and a test run using a companion 1.5 cm x 1.5 cm "bulk" Si(211) substrate to ensure that the growth recipe was optimized for those sample mounting and heating conditions.

The M2000 SE system was used to monitor all sample heating and epitaxial layer growth processes in the MBE system. We found this capability to be indispensable for evaluating the characteristics of the "compliant" layer during heating and for assessing the growth of the ZnTe and CdTe layers in real-time.

Ellipsometry data that illustrate the substrate heating and ZnTe/CdTe growth profile on a Si(211) "compliant" layer are presented in Figure 2.24. This figure gives the ellipsometric parameter, psi, at a single spectral channel (2.5 eV) as a function of time during heating of the "compliant" layer and growth of the II-VI epilayers on the thin Si(211) substrate. All of the principal features in the heating and layer growth process are evident in the psi data. Over the period from approximately 45 to 60 minutes the sample temperature is ramped from 200°C to 550°C to desorb the H passivation layer from the Si(211) substrate. The temperature is then ramped back down for subsequent growth of the ZnTe and CdTe layers.

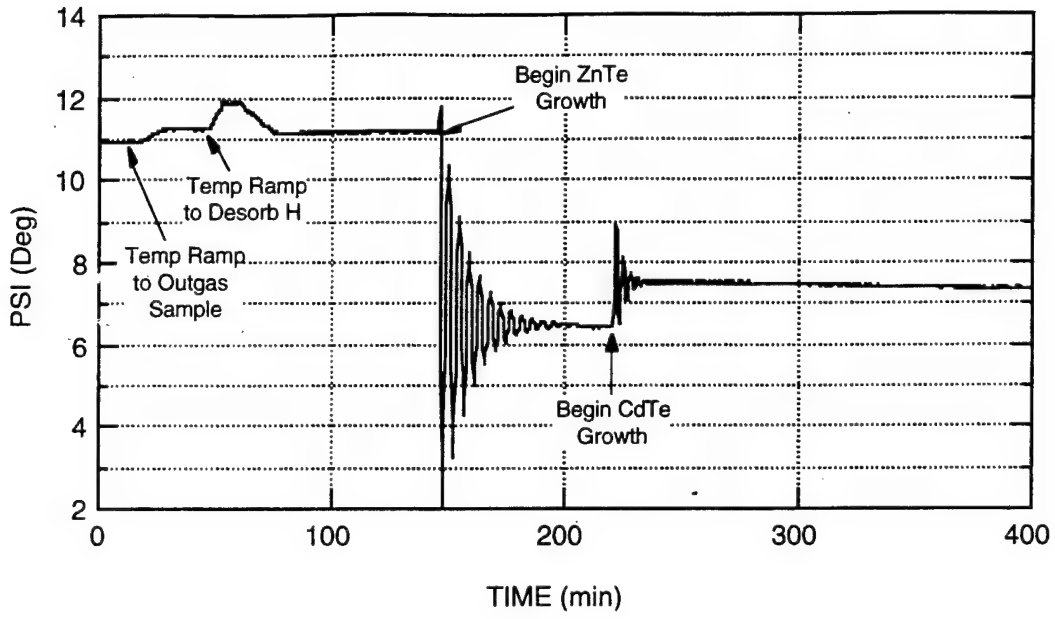
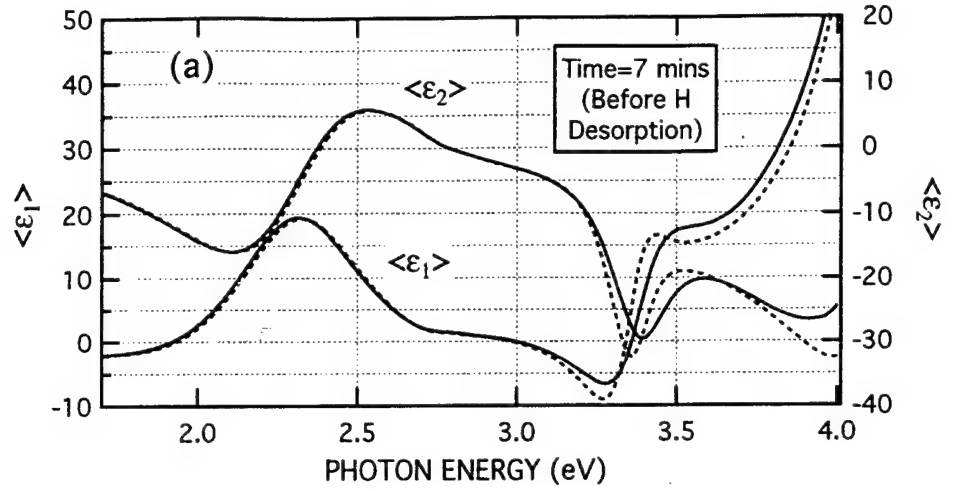
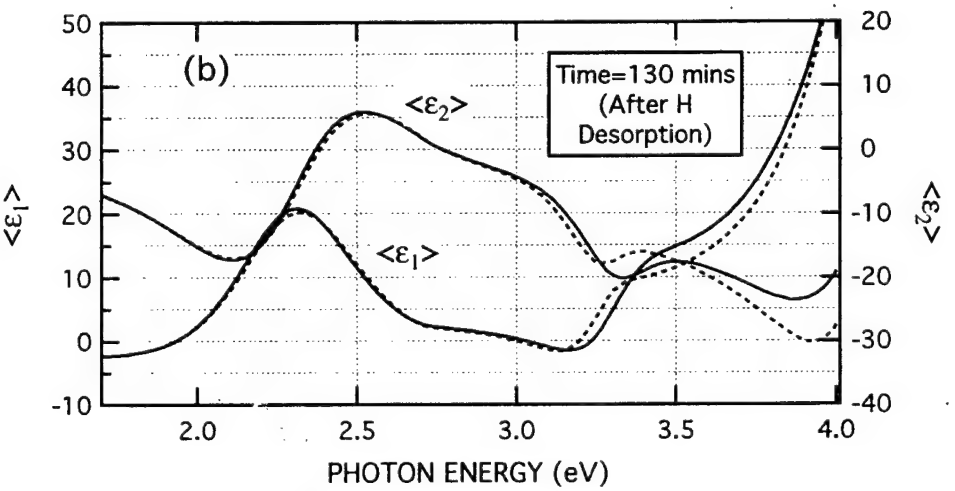


Figure 2.24. Ellipsometric parameter "psi" at 2.5 eV during substrate heating, hydrogen desorption, ZnTe deposition and CdTe deposition.

Before we conducted these experiments we had a serious concern about the fate of the ultra-thin Si(211) layer during the high temperature hydrogen desorption step. Specifically, we were concerned that the thermal stress might cause the Si(211) layer to delaminate or fracture during the heating or cooling sequence. However, the data in Figure 2.24 show no evidence of layer lift-off or degradation during the heating cycle. This is reinforced in Figure 2.25 by the pseudo-dielectric function data (ε_1 and ε_2) and model fits over the range from 1.7-4.0 eV acquired before and after H desorption (t=7 min and 130 min, respectively). The quality of the experimental data and the agreement between those data and the model fits reveal that the Si(211) compliant layer is *fully intact* and that the layer thickness is essentially unchanged after heating. The slight differences between the experimental data in (a) and (b) are due to the differences in substrate temperature at the two data acquisition times (~100°C and ~250°C).



Si(211)	56 Å
SiO_2	2302 Å
Si(100)	Substrate



Si(211)	54 Å
SiO_2	2305 Å
Si(100)	Substrate

Figure 2.25. Pseudo-dielectric functions (ε_1 and ε_2) and model fits for "compliant" Si(211) layer thickness before and after high temperature H desorption step. (a) shows data and fit at t=7 min (temp about 100°C) prior to H desorption—Si(211) layer thickness from model fit = 56 Å. (b) shows data and fit at t=130 min (temp approximately 250°C) after 550°C H desorption—Si(211) layer thickness from model fit = 54 Å.

Figure 2.26 shows the *in situ* pseudo-dielectric function data over the spectral range from 1.7 to 4.2 eV and model fits to those data for a 6 μm-thick CdTe layer grown on a 56 Å thick Si(211) "compliant" layer. The excellent agreement between the model fit and the experimental data show that the CdTe layer grown on the compliant substrate has optical properties that are virtually identical to those obtained from CdTe layers grown on a conventional substrate.

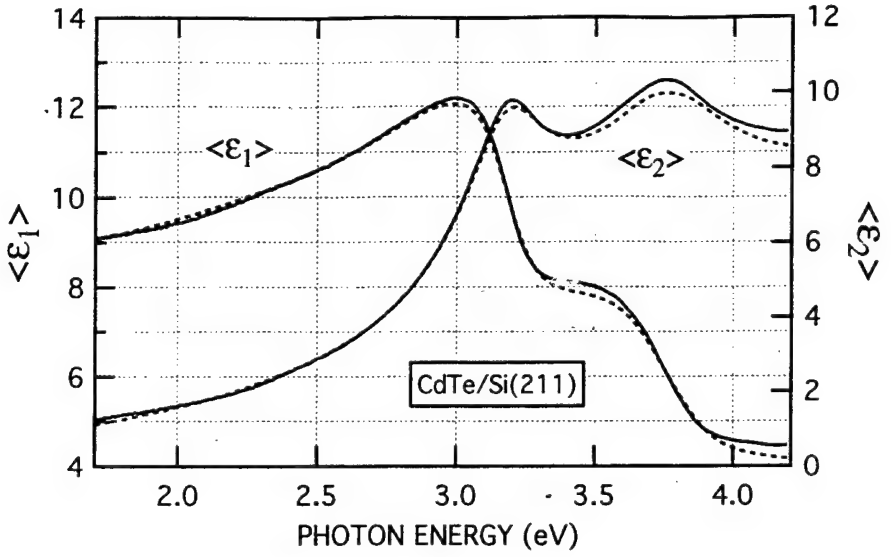


Figure 2.26. Pseudo-dielectric functions (ε_1 and ε_2) and model fits for thick (6 μm) CdTe layer grown by MBE on Si(211) "compliant" substrate.

The surface morphology, surface dislocation density, and crystallinity of the CdTe layer are given by the Nomarski micrographs and x-ray DCRC data in Figure 2.27. The surface morphology is comparable to that obtained for layers grown on bulk substrates (Figure 2.23) and on layers grown on SIMOX and wafer-bonded substrates. The surface dislocation density (EPD) measured on the CdTe/ZnTe/"compliant" Si(211) sample (2.7×10^6 cm^{-2}) is also comparable to that measured on the CdTe/ZnTe/"bulk" Si(211) sample (2.2×10^6 cm^{-2}).

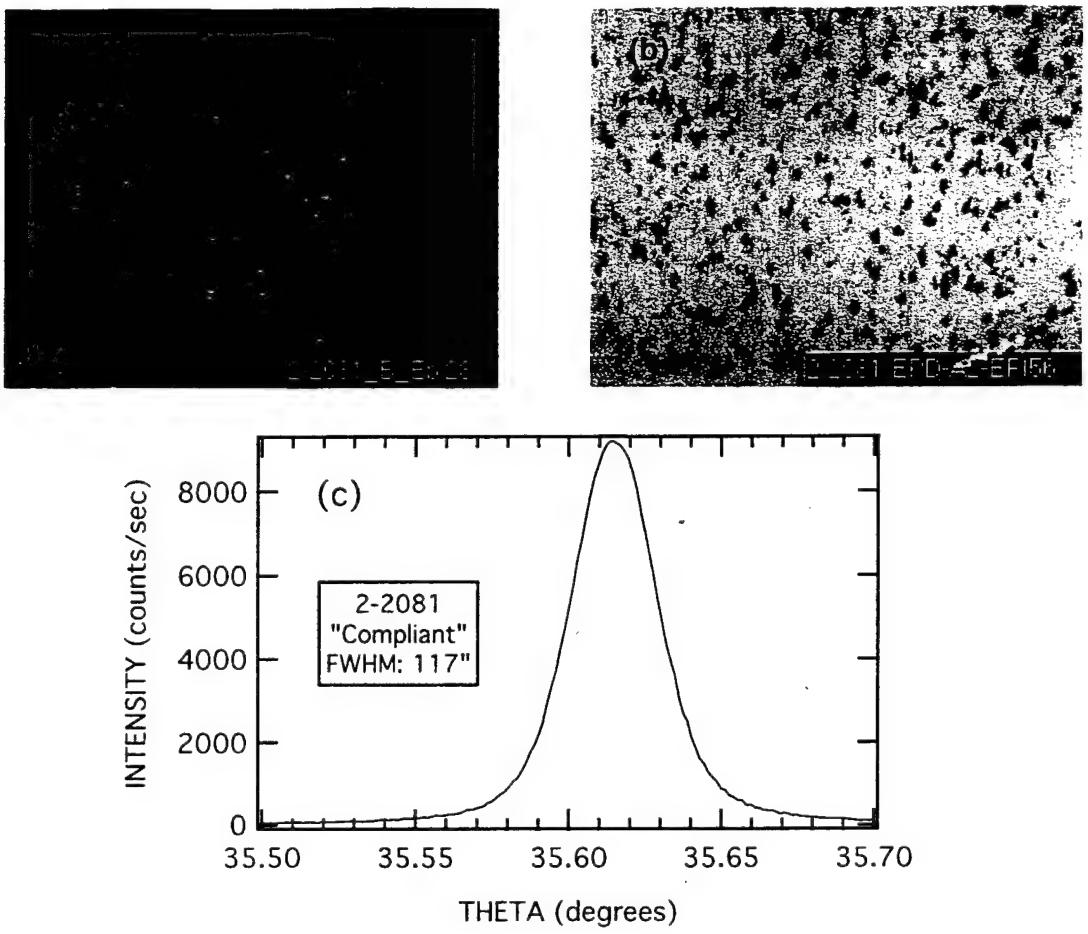


Figure 2.27. Surface morphology and structural quality of 8μm-thick CdTe layer grown on 58Å thick Si(211) "compliant" substrate: (a) Nomarski micrograph of CdTe surface; (b) micrograph after defect etching to reveal surface dislocations (EPD: 2.7×10^6 cm^{-2}; (c) x-ray DCRC (FWHM: 117 arc-sec).

Although MBE growth of CdTe on the "compliant" substrates produced layers with structural and defect properties comparable to those obtained on thicker Si(211) substrates, we observed *no evidence* of "compliancy" and the attendant reduction in CdTe defect density or defect accommodation by the thin Si(211) layer. This corroborates the conclusion reached in the III-V materials studies on this program – i.e., insofar as the quality of MBE layers grown on the thin substrates is an acceptable indicator, growth on the "compliant" layers *does not* result in a reduction or redistribution of dislocations in the epitaxial layer. Although it is inappropriate to conclude solely from these studies that the concept of substrate "compliancy" is totally untenable, our studies suggest that, at least for the materials systems investigated here, it is a notion that lacks firm support from either theory or experimental observations.

A final series of MBE growth runs was performed to examine whether high quality HgCdTe films could be nucleated and grown directly on the thin Si(111) "compliant" substrate. Growth of HgCdTe on "standard" Si(211) substrates requires the growth of intervening ZnTe and CdTe layers to provide a template for subsequent growth of the HgCdTe layer. Direct nucleation and growth of a HgCdTe layer would be a demanding test for the ability of the thin "compliant" substrate to moderate defect formation propagation in the II-VI layer.

The selective absorption of substrate IR heater radiation by the narrow bandgap HgCdTe layer makes it impractical to use 'free-mounting" and radiant heating of the substrate for HgCdTe growth in our MBE system. For these experiments the substrate was thermally contacted to a solid graphite fixture using a colloidal graphite slurry ("DAG"). In this configuration, radiation from the heater is absorbed by the graphite block, and the heat is conductively transferred to the substrate by the DAG layer. This mounting and heating geometry eliminates the thermal control problem that arises during radiant heating of a narrow bandgap layer. However, even though this process is routinely used for growth of high quality HgCdTe layers on II-VI substrates (e.g. CdZnTe), we later found that it is not well-suited for II-VI growth on Si. An important difference between growth on Si and growth on CdZnTe is that a high temperature step (550°C) is required for desorption of the H passivation layer from the Si surface. At that temperature, the DAG layer fractures and the substrate delaminates from the holder, thereby breaking the thermal conduction pathway and causing severe temperature non-uniformity across the substrate.

We performed growth runs on both bulk Si(211) (with ZnTe/CdTe buffer layers) and on compliant layers using this approach, and in both cases the resulting HgCdTe layers were polycrystalline and had a rough surface morphology. Figure 2.28 shows the variation in the ellipsometric parameter, psi, during hydrogen desorption and HgCdTe growth on a bulk Si(211) sample contacted with DAG to a graphite holder. The thermal cycle required for H desorption is evident from the change in psi during the first 75 minutes. Growth of the HgCdTe layer is initiated at about 115 min, and the oscillations in psi with time indicate that material is being adsorbed on the Si surface. Although the SE signal does not show direct evidence for sample delamination during H desorption, the downward drift in the data during HgCdTe growth is a clear indicator of non-ideal growth. Sample delamination was apparent when the sample was examined after removal from the MBE system.

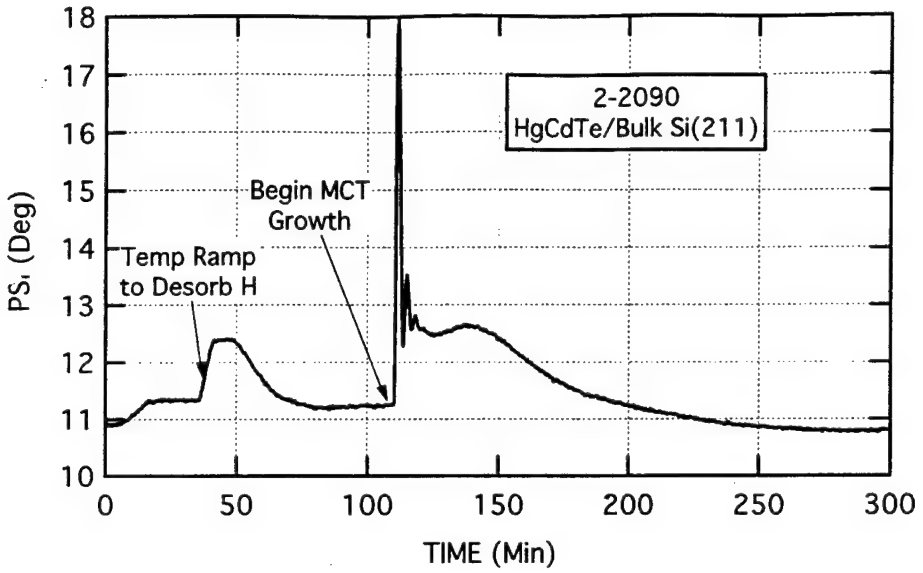


Figure 2.28. Time evolution of psi during H desorption and direct HgCdTe growth on a bulk Si(211) substrate DAG-mounted to a graphite holder. Sample delamination during H desorption results in spatial non-uniformity in temperature which causes surface roughening and formation of a polycrystalline HgCdTe layer.

We attempted to overcome the substrate delamination problem in a series of experiments in which we used radiant heating to desorb the hydrogen followed by deposition of a thin (1000Å) tellurium "capping" layer to protect the free Si surface. The sample was then removed from the MBE chamber and mounted to a solid graphite holder using DAG. The sample was re-introduced into the chamber and then heated to desorb the Te layer, exposing the free Si surface for subsequent epitaxy. Although this process allowed us to overcome the substrate delamination problem, the MBE-grown HgCdTe layers were also polycrystalline and had a rough surface morphology.

We believe that the failure to obtain a single crystal layer using this method is not necessarily related to a problem with II-VI nucleation on the Si surface. Instead, we believe that it is associated with the formation of a thin disordered layer during interaction of Te atoms with the Si surface, resulting in a poor template for single crystal epitaxial growth. The direct nucleation of HgCdTe on a Si substrate could overcome the difficulties inherent in growth of CdTe by MBE, and therefore remains an important objective. We plan to continue follow-on investigations to further explore the surface preparation and sample heating procedures required to produce a high quality template for direct HgCdTe nucleation on silicon.

2.2.4 Characterization of Growth Mode and Defect Structure In II-VI Layers on Si(211) Substrates

As an adjunct to the studies of II-VI epitaxy on thin "compliant" layers, we investigated in greater detail the defect characteristics of HgCdTe layers grown on conventional Si(211) substrates. This not only provides a solid reference point for comparison of the "compliant" substrate results, but it also offers insight into an observation that we have found to be surprising and interesting: namely the diminution in density of threading dislocations (TDs) by three orders of magnitude between the initial ZnTe/Si(211) substrate and the HgCdTe device layer. We initiated a careful TEM characterization of the TD density in II-VI epilayers of CdTe and ZnTe grown on bulk Si(211), and we found that the TD density is below 10^6 cm^{-2} at the surface of a 6 μm-thick CdTe layer grown on top of 1 μm of ZnTe on Si(211). For example, the plan view micrograph presented in Figure 2.29 contains *no threading dislocations*, and a second micrograph from a different region showed only one TD.

Figure 2.29. Plan-view TEM micrograph of a 6 μm-thick CdTe epitaxial layer grown on a 1μm-thick ZnTe layer on a bulk Si(112) substrate.

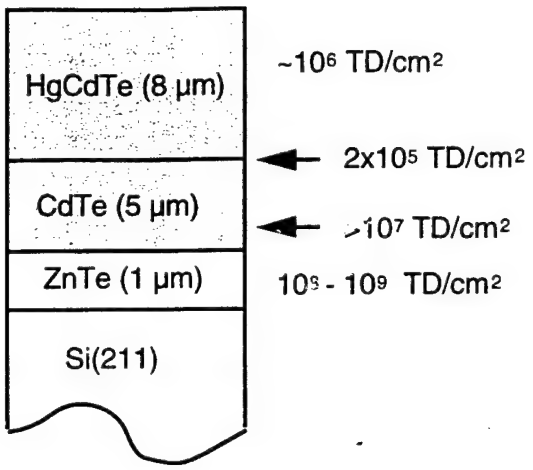


Figure 2.30. Schematic illustration of HgCdTe-on-Si(211) structure, inclucing approximate number of threading dislocations at different positions in structure.

The change in the density of threading dislocations in a typical HgCdTe-on-Si device structure is shown in Figure 2.30. The TD density in the CdTe layer is initially high near the ZnTe/CdTe interface ($>10^8$ cm^{-2}), as expected for the 12% lattice mismatch between the ZnTe layer and Si substrate, but it decreases rapidly with film thickness and reaches a relatively constant minimum value within 2 μm from the interface. The TD density in the remainder of the film is amazingly low, considering the large lattice mismatch between CdTe and ZnTe (≈ 6%) and the overall 19% mismatch between CdTe and the Si substrate. Evidently TDs either annihilate each other in the CdTe layer, or are caused to bend over such that they don't propagate vertically into the remainder of the layer. Given what is known about similar behavior in III-V semiconductors, and the properties of CdTe, this large reduction in TD density was entirely unexpected.

An understanding of the mechanisms responsible for such significant annihilation of threading dislocations in II-VI's would be potentially valuable toward reducing the TD density in other systems. Toward this goal, we conducted preliminary studies on the initial sources of TD formation, with emphasis on the early stages of epitaxy in the highly mismatched ZnTe/Si and CdTe/ZnTe systems. We prepared a set of ZnTe-on-Si(211) samples with ZnTe thickness of 50Å, 200Å, and 500Å. Prof. J. Speck and co-workers at UCSB analyzed the structural characteristics of the layers using cross-sectional transmission electron microscopy and atomic force microscopy. Figure 2.31 shows cross-sectional TEM images of the ZnTe/Si(211) interface region for the three samples, and Figure 2.32 shows a higher resolution TEM image of a portion of the ZnTe layer in the 50Å sample.

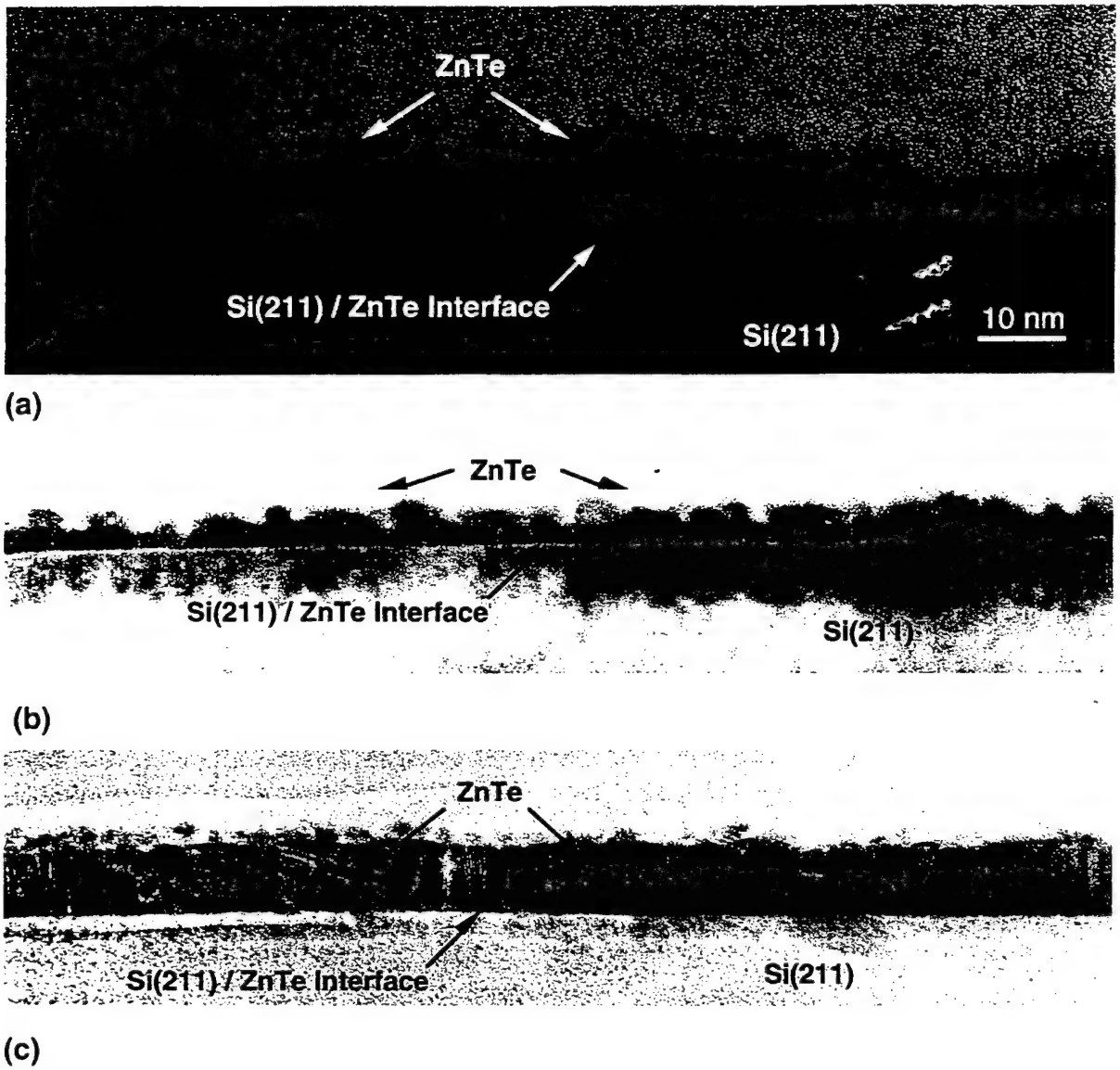


Figure 2.31. Cross-sectional TEM micrographs showing the region near the interface between the ZnTe MBE layer and the Si(211) substrate for ZnTe layer thicknesses of 50Å (a), 200Å (b), and 500Å(c).

The sequence of micrographs in Figures 2.31 and 2.32 indicate that ZnTe (a=6.10 Å) initially forms 3-dimensional islands on the Si(211) substrate (a=5.43 Å) with varying heights and different degrees connectivity between adjacent islands. As MBE proceeds, the islands coalesce into a fully connected layer (Fig. 2.31b) with surface roughness that decreases with increasing layer thickness (Fig. 2.31c). This interpretation has also been confirmed using atomic force microscopy (AFM).

The data are consistent with a 3-D (Volmer-Weber) mode for crystal growth. This growth mode occurs when the interaction energy of the deposited atoms with the substrate is less than the

energy that the deposited atoms would have on their own substrate. This model can be used to describe the general features of the growth process, but it does not provide detailed information about the origin and migration of dislocations within the growing layer. A detailed analysis of the TEM data shows evidence that threading dislocations form at the intersections between separate islands when they grow together. However, it is not known whether these TDs are the same ones observed throughout the film in the later stages of growth, or whether new TDs form due to some other mechanism.

These results demonstrate the primary role of the ZnTe layer in these structures is to provide a lattice constant "stepping layer" for the subsequent growth of CdTe (a = 6.48 Å) and HgCdTe. That is, the intermediate ZnTe layer is important for maintaining epitaxial orientation in the growth stack. However, it appears that the low threading dislocation densities in the CdTe are achieved through thickness alone. It is possible that by understanding the origin of the TDs observed in thick layers, it may be possible to speculate on mechanisms of TD annihilation, and eventually to discover methods to manipulate these mechanisms experimentally. If this were possible, it would potentially be a breakthrough result relevant to all forms of heteroepitaxy.

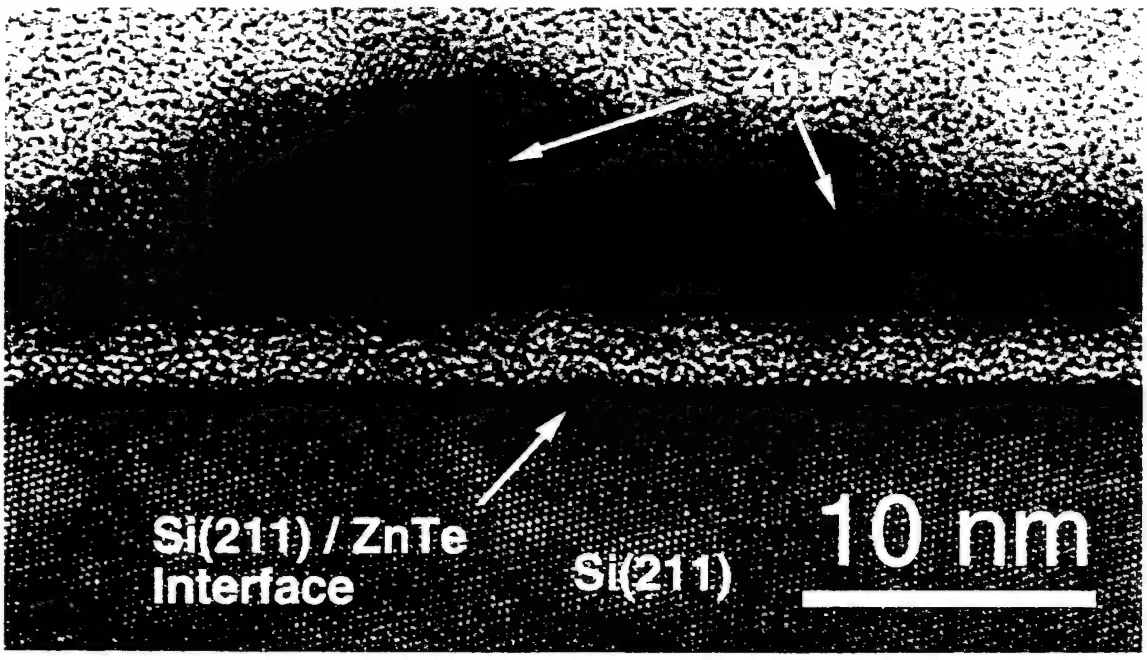


Figure 2.32. High-resolution x-TEM image showing of a magnified portion of the interface region in the sample containing the 50Å-thick ZnTe layer.

2.3 RELAXATION MECHANISMS AND COMPLIANCY IN HETEROEPITAXY

In an attempt to rationalize some of the existing literature reports of unusual behavior during growth of mismatched epilayers on bonded thin-film "compliant" substrates, and to clearly articulate the possible modes of thin-film strain relaxation during heteroepitaxy, the basic principles governing the distribution and evolution of strain in such systems was considered from a solid mechanics perspective. This analysis showed that the popularly held belief that large-scale elastic relaxation can occur in an epitaxial film deposited onto a thin second film that is bonded to a third, thicker substrate is unrealistic when all the layers remain solid, because the requirements that the film be attached robustly to the underlying thick substrate and simultaneously be free to slide over the substrate are mutually inconsistent. However, if the film is initially under compression and is attached to a viscous medium, such as a low-viscosity oxide at high temperatures, it is possible for the film to relax elastically through buckling. This has been observed experimentally at temperatures above 800°C for SiGe bonded to BPSG. Over limited areas, it is possible to obtain relatively flat, relaxed layers via this mechanism, however it is unlikely to be extendable to larger areas or to the much lower temperatures needed for III-V or II-VI epitaxy.

The most common mode of strain relaxation in heteroepitaxy is through plastic or dislocation-mediated processes. In the ideal case, under growth conditions that favor the formation of a continuous, planar, and coherently strained epilayer, once the accumulated stress due to the film being strained to a different lattice constant reaches a sufficiently high value, dislocations will nucleate and move through the film in a manner that completely relieves the stress induces reorganization of atom locations required to accommodate the change of in-plane lattice spacing without leaving any residual defects. In real materials, dislocations generally cannot move freely through the crystal without some hindrance, and many become immobilized, trapped, or blocked in their motion. This can result in incomplete relaxation, but more importantly, can leave a residual remnant population of threading dislocations that may continue to propagate into subsequently grown layers.

It is crucial to understand that aside from extrinsic dislocations that form due to impurities or macro defects, the majority of dislocations in an otherwise high quality single crystal film are generated in response to strain in a layer; i.e., to physical deformation of the layer relative to its natural state in the absence of stress. If a layer is not physically deformed by being non-uniformly stretched, compressed, bent, or heated, there is no force acting to generate or move dislocations. This is important in understanding why "twist-bonding" of the thin "compliant substrate" cannot actually operate in real samples. It has been proposed that a growing epitaxial film deposited onto a second thin layer that is bonded to a thick substrate crystal (and possibly twisted relative to the underlying wafer), might be able to effectively relax elastically through the

plastic deformation of the underlying thin layer. The basis for this notion originated with the concept of growth of a film on a second, free-standing layer that is totally free to move in the plane of the film, and various calculations of the partitioning of stress and strain in such a situation have been presented. However, the extension of this behavior to the case of a bonded film is totally inappropriate unless the film is free to slide on the underlying thick substrate. Because unless it can do so, there can be no buildup of strain in the thin layer, and hence no force that acts to generate dislocations. All or nearly all of the dislocation formation and movement will still take place in the top layer since it is the only entity that is actually strained. Our calculations have shown that the only place where an actual shear stress exists in the intermediate (bonded) thin layer is at the edge of the film, where a free vertical surface is present. This stress only penetrates laterally into the main film region by a distance equivalent to one or two film thicknesses, and therefore cannot be effective in mediating the relaxation of the thin layer over useful distances in a uniform structure.

Consideration of these issues leads to the following conclusions about possible routes to achieve relaxation of a strained film under conditions of two-dimensional, coherently strained growth: if the film is supported on a layer the viscosity of which can be sufficiently reduced, a local form of elastic relaxation is possible, in which the film either buckles, it is attached over a large area, or expands uniformly if its lateral extent is sufficiently small relative to the viscous drag of the underlying layer. In the case of buckling, viscous flow of the underlying material accommodates the peaks and troughs of the buckled morphology. It is highly unlikely that any form of film/substrate attachment that involves even sparse attachment via solid-solid chemical bonds can provide the degree of interfacial sliding originally envisioned by proponents of the twist-bonded approach to compliancy. Plastic relaxation via dislocation-based processes originating in the epitaxial layer itself appears to be the most likely mode of strain relief in most semiconductor systems of current interest. This means that the most effective strategies for reducing or eliminating the population of remnant threading dislocations in such a layer will be based on reducing the density of threading dislocations and removing the barriers to dislocation motion that would in the ideal case allow the film to fully relax to a defect-free state. As discussed below, there are two recently experimental results that suggest that the necessary degree of dislocation movement and/or self-annihilation is actually possible in semiconductor systems of real practical interest.

In recent experiments on lateral oxidation in III-V heteroepitaxial structures, Chavarkar *et al.* observed that nearly complete relaxation of coherently-strained and partially-relaxed InGaAs layers is achieved during oxidation of an underlying layer of AlAs, without the formation of a large population of residual threading dislocations. It is postulated that the local strain produced in the vicinity of the passing oxidation front increases the formation and motion of strain-reducing edge dislocations and also reduces any barrier to dislocation motion that would

otherwise prevent the necessary linear extension of misfit dislocations at the film bottom interface. It is also possible that the oxidation process continuously consumes interfacial misfit dislocations, thereby allowing the formation and glide of additional stain-relieving dislocations to occur more readily. Understanding the details of dislocation dynamics in this type of system should provide invaluable clues about how to actively influence and guide the necessary dislocation behavior in more general heteroepitaxy scenarios in order to achieve an equivalent result without the necessity of employing lateral oxidation *per se*.

The other class of observations that bears favorably on the possibility of understanding and controlling dislocation plasticity in the heteroepitaxy context is the dramatic reduction in TD density observed in thick buffer layers of CdTe grown by MBE on Si. (As discussed in the previous section, the CdTe is actually grown on top of a previously grown layer of ZnTe, which serves to establish twin-free, single-orientation growth.) It is clear that in this material system, which is characterized by very large lattice mismatch (6.2% between the CdTe and ZnTe layers), the movement of threading dislocations in the CdTe must be very facile, even at the rather low growth temperatures that are employed in MBE (270-320°C). The specific reasons for enhanced dislocation motion and threading dislocation reduction in this system are currently not known, but we believe that through systematic experiments to capture the state of the film at various stages in the epitaxial growth process, the behavior can be understood and the underlying mechanisms can be elucidated. This understanding should subsequently lead to the ability to directly modify dislocation dynamics during plastic relaxation. This capability could be exploited to greatly expand the range of materials that can be grown heteroepitaxially with sufficient crystal quality for microelectronic applications.

Based on the lack of promising results in "compliant substrates", two new models for strain relaxation were developed. In the first modeling effort, we developed the concept of "*relaxation enhancing interlayers*". These interlayers correspond to layers that maintain the structural stability of the heteroepitaxial layer stack, but enhance relaxation by removing the locally highly strained region associated with misfit dislocations. In real systems, these layers could correspond to either low viscosity glasses, such as being developed at NRL, or porous layers, such as realized by lateral oxidation of high Al-content III-V layers. The reduction of the local stresses by the interlayers eliminates the blocking effect of misfit dislocations and allows efficient motion of threading dislocations with consequent overall strain relaxation in the heteroepitaxial film. An analytical model was developed that quantitatively described the dislocation density changes during growth with relaxation-enhancing interlayers. The full results of this work appeared recently in a paper in the *Journal of Electronic Materials* (see Reference 1 in Publications Section).

In the second modeling effort, we developed a comprehensive and novel description for the origin of the cross-hatch surface morphology. This morphology is commonly observed in strain-relaxed layers that grew in a Frank van der Merwe mode (planar growth). We demonstrated that both strain relaxation associated with misfit dislocation formation and lateral surface step flow are required for the appearance of mesoscopic scale surface undulations during layer growth. The results of Monte Carlo simulations for dislocation-assisted strain relaxation and consequent film growth predict the development of cross-hatch patterns with a characteristic surface undulation magnitude of 50 Å in an approximately 70% relaxed $In_{0.25}Ga_{0.75}As$ layers. This was supported by AFM observations of cross-hatch morphology in the same composition samples grown well beyond the critical thickness for misfit dislocation formation. The full results of this work appeared recently in a paper in *Applied Physics Letters* (see Reference 2 in Publications Section).

Section 3
SUMMARY AND CONCLUSIONS

Experimental and theoretical modeling studies were conducted to examine several routes for achieving low threading dislocation densities through substrate "compliancy". The potential use of ultra-thin (<60Å) "compliant" layers as substrates for mismatched heteroepitaxy was investigated in two technologically important semiconductor materials systems: InGaAs-on-GaAs and CdTe-on-Si(211). These studies indicate that contrary to claims made earlier by Lo and co-workers and Lin *et al* in work conducted in III-VI semiconductor layers, large-area elastic relaxation is highly *unlikely* to occur in these films except in systems where the underlying layers have extremely low viscosity. The salient results from our research on both systems are summarized below.

3.1 InGaAs COMPLIANT LAYERS ON GALLIUM ARSENIDE

Lin and co-workers at the University of Houston and AOI, Inc. interpreted the improved performance from semiconductor lasers grown on InGaAs "compliant" layers as the result of defect reduction in the active layer due to lattice accommodation by the "compliant" InGaAs substrate. In addition, they reported that changes in the RHEED pattern during heating of the InGaAs/GaAs structure in a high vacuum (MBE) environment provided direct evidence for structural alterations of the "twist-bonded" layer. To examine this latter point further, we conducted a study of the structure and surface properties of InGaAs/GaAs "compliant" layers before and after heating in a III-V MBE system. The objectives of the work were to examine in detail any possible structural changes in the thin InGaAs layer and to investigate whether additional layers epitaxially grown on the "compliant" layer would exhibit reduced defect density compared to identical films grown on conventional substrates.

The diagnostic techniques employed in this study included TEM, RHEED, Auger depth profiling, and *in situ* and *ex situ* spectroscopic ellipsometry (SE). We verified the existence of a thin (~55Å) InGaAs layer on the GaAs surface before heating, and we confirmed that the surface structure did indeed change upon heating prior to epitaxy. However, our analysis showed that in all cases, the thin InGaAs "compliant" layer did not survive heating to temperatures needed for surface oxide desorption prior to MBE growth. It was clear that the observed changes in the InGaAs "compliant layer" resulted simply from delamination of the layer from the substrate and *were not due to structural rearrangement of the InGaAs layer.* Because our analysis showed that the thin InGaAs layer was either entirely missing or existed only in fragments on the GaAs surface, subsequent growth experiments were not pursued. Based on these and other findings, we conclude that the results reported by Lin *et al.* can be explained in terms of sample delamination rather than changes in lattice structure due to substrate "compliancy".

It is important to note that a negative result of this kind does not entirely discredit the 'twist-bonded' compliant substrate concept. However, these findings certainly support the more widely held position within the materials science community that many earlier reports of compliant substrate behavior were largely based upon misinterpretations of experimental data. We strongly feel that the conditions requiring a film to be attached robustly to a thick substrate, while simultaneously being free to slide over the substrate *in the solid phase*, are mutually inconsistent, and we therefore conclude that the notion of compliancy via large-scale elastic relaxation in an ultra-thin layer is untenable.

The results obtained in our work and from other recent investigations on heteroepitaxy in highly mismatched systems support the more conventional mechanism of strain relaxation through dislocation-mediated processes that induces plastic relaxation within the epitaxial layer. In that context, a successful defect reduction strategy would involve the elimination of energy barriers to dislocation motion, which in turn would facilitate full relaxation of the film. For example, relaxation via dislocation plasticity is a mechanism that has been shown by J.S. Speck and co-workers to be consistent with the observation of very low threading dislocation densities ($<10^6\,cm^{-2}$) in some classes of relaxed heteroepitaxial films. They have developed a model that relies upon "relaxation-enhancing interlayers" that maintain the structural stability of the heteroepitaxial layers but enhance relaxation by removing the locally strained region associated with misfit dislocations. The reduction of these local stresses eliminates the blocking effect of misfit dislocations and allows efficient motion of threading dislocations with the attendant relaxation of strain in the heteroepitaxial film. Reference 1 (Publications Section) provides a full description of the model and of the changes in dislocation density due to presence of relaxation-enhancing interlayers during growth.

The experimental results and conclusions described above concerning the lack of "compliancy" in the InGaAs-GaAs system were obtained within the first 18 months of the present program. After discussing alternative prospects for research in this field with the DARPA Program Manager (Dr. William Coblenz) and the Air Force Contract Monitor (Maj. Daniel Johnstone), we redirected the program to emphasize studies of "compliant substrate" behavior in II-VI materials grown on thin Si(211) layers on Si(100), a materials system of critical importance to the high performance infrared detector community.

3.2 II-VI EPITAXY ON SILICON COMPLIANT LAYERS

The principal objectives of this component of the program were to characterize the properties of ultra-thin "compliant" Si(211) layers bonded to oxidized Si(100) substrates and to investigate the structural and defect characteristics of CdTe and HgCdTe films grown on the "compliant" layers. The properties of the II-VI films grown by MBE on the "compliant" layers were compared with the properties of films grown on substrates having considerably thicker Si(211) layers formed by the SIMOX process (1500 Å Si(211)/Si(211)) and by wafer bonding (2 μm Si(211)/Si(100)) to assess the effect of substrate film thickness on II-VI layer quality.

After conducting multiple process iterations to develop and optimize the wafer bonding and layer growth procedures, Si "compliant substrate" samples comprising thin (<60Å) Si(211) layers intimately contacted to oxidized Si(100) substrates were successfully fabricated using wafer-bonding and selective etching methods. This work was performed in collaboration with Dr. Karl Hobart and co-workers at the Naval Research Laboratory and with several commercial vendors. A comprehensive series of spectroscopic ellipsometry investigations were performed to assess the Si(211) layer thickness and stability in response to various surface treatments that included *ex situ* etching and surface passivation, and *in situ* heating and epitaxy in a II-VI MBE system. The following summarizes the principal results from our investigation of the ultra-thin Si(211) layers and the quality of the MBE-grown CdTe layers grown on those substrates.

- The 56 Å Si(211)-on-Si(100) "compliant" layers were robust and stable against all *ex situ* etching and surface passivation steps required for preparation of the sample for II-VI MBE.
- The thin Si(211) layers were stable during all heating cycles and II-VI layer growth procedures in the MBE system. Approximately 10 MBE growth runs were conducted using these substrates and neither layer delamination nor detectable layer degradation was observed in any of the samples.
- 8 μm-thick CdTe layers on 1 μm-thick ZnTe layers were grown on the "compliant" substrates. The surface dislocation densities (EPD: 2.7 $x10^6$ cm^{-2}) and x-ray double-crystal rocking curve FWHM (117 arc-sec) were comparable to the EPDs and DCRC results in samples grown on bulk Si(211) substrates (2.2 $x10^6$ cm^{-2} and 80 arc-sec, respectively).
- CdTe layers grown on the 1500 Å thick Si(211) layers formed by the SIMOX process and on the 2 μm-thick Si(211) layers wafer-bonded to oxidized Si(100) substrates gave EPD counts and x-ray DCRC results comparable to those obtained for layers grown on bulk Si(211) substrates.
- Direct nucleation and growth of HgCdTe (with no intervening CdTe layer) on either the "compliant" substrates or the "standard" substrates resulted in HgCdTe layers with poor crystalline quality and high defect density. This is consistent with results previously obtained in our laboratory.

- To the extent that defect density, crystallinity, and optical characteristics of the II-VI layers grown on the 56 Å thick surface can be used as indicators, *we found no evidence for "compliancy"* during MBE. The structural and optical characteristics of II-VI layers were essentially indistinguishable from layers grown on bulk or wafer-bonded substrates.

The lack of observed "compliant behavior" notwithstanding, the excellent structural properties obtained for the II-VI layers grown on the 56 Å thick Si(211) "compliant" layers on Si(100) and on the 2 μm-thick wafer-bonded Si(211)/Si(100) substrates are particularly important because they provide the experimental basis for growth of high quality HgCdTe infrared detector layers on Si(100). Although HgCdTe detector layers were not actually grown on the 8 μm-thick CdTe layers, there is no reason to believe that the detector performance in such layers would not be comparable to performance achieved in HgCdTe detectors grown on bulk Si(211). To our knowledge, this is the first demonstration of an especially critical step in achieving monolithic integration of HgCdTe detector structures readout ICs fabricated in Si(100) substrates, namely growth of a high quality II-VI layer on a Si(211) layer intimately contacted to a Si(100) substrate. We feel that this technology could enable the elimination of indium "bump-bonding" methods for contacting the detectors to the readout structures, thereby reducing device complexity and increasing the reliability of IR focal plane arrays fabricated in HgCdTe.

In addition to investigating compliant substrate behavior in II-VI layer growth, we conducted a cursory study of the formation of threading dislocations II-VI layers grown on Si(211) substrates and the dependence of the defect density on II-VI layer thickness. Specifically, we performed a cross-sectional TEM analysis of ZnTe layers of different thicknesses grown on Si(211)substrates to provide insight into the intriguing observation of a large reduction in threading dislocation density between the initial ZnTe/Si interface and the interface between the subsequently grown CdTe layer. (ZnTe is a lattice mismatch-accommodating "passivation" layer routinely grown prior to CdTe deposition). We found that ZnTe initially forms 3-D islands, and that as MBE proceeds, the islands coalesce into a fully connected layer with progressively decreasing surface roughness. The observations are fully consistent with a 3-D Volmer-Weber growth model. The TEM data reveal the formation of threading dislocations at the boundaries between the connected islands. However, insufficient data are available from this preliminary study to link the formation of the high density of TDs in the thin ZnTe layers with the reduced defect density in thicker layers. This requires a much more comprehensive TEM study of multiple layers. The provocative result that the defect density decreases by as much as three orders of magnitude from the initial ZnTe/Si(211) interface to the top of the CdTe layer remains unexplained. However, we believe that elucidating the mechanism(s) for defect annihilation with increasing layer thickness in largely mismatched systems is of considerable general importance for heteroepitaxy in a wide range of systems, and we recommend that DARPA support future programs that focus explicitly on this important issue.

PUBLICATIONS

The two technical publications stemming from this research effort are listed below. In addition, a manuscript is being prepared on the epitaxial growth of II-VI semiconductors on thin Si(211) layers on Si(100) substrates.

1. A.E. Romanov and J.S. Speck, "Relaxation Enhancing Interlayers (REIs) in Threading Dislocation Reduction", *J. Electron. Mater.* **29**, 901-905 (2000).

2. A.M. Andrews, A.E. Romanov, J.S. Speck, M. Bobeth, W. Pompe, "Development Of Cross-Hatch Morphology During Growth Of Lattice Mismatched Layers," *Appl. Phys. Lett.* **77**, 3740 (2000).